ST7781R

240RGB x 320 dot 262K Color with Frame Memory Single-Chip TFT Controller/Driver

Datasheet

Version 1.0
2010/09

Sitronix Technology Corporation

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1 GENERAL DESCRIPTION

The ST7781R is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 720 source line and 320 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts, 8-bits/9-bits/16-bits/18-bits parallel interface. Display data can be stored in the on-chip display data RAM of 240x320x18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with the fewest components.

2 FEATURES

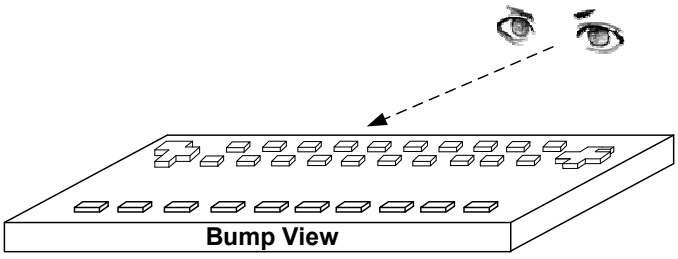
- Single chip TFT-LCD Controller/Driver with On-chip Frame Memory (FM)
- Display Resolution: 240*RGB (H) *320(V)
- Frame Memory Size: 240 x 320 x 18-bit = 1,382,400 bits
- LCD Driver Output Circuits
  - Source Outputs: 240 RGB Channels
  - Gate Outputs: 320 Channels
  - Common Electrode Output
- Display Colors (Color Mode)
  - Full Color: 262K, RGB=(666) max., Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- Programmable Pixel Color Format (Color Depth) for Various Display Data input Format
  - 12-bit/pixel: RGB=(444) using the 1.38M -bit frame memory
  - 16-bit/pixel: RGB=(565) using the 1.38M -bit frame memory
  - 18-bit/pixel: RGB=(666) using the 1.38M-bit frame memory
- MCU Interface
  - Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit & 18-bit)
  - 6/16/18 RGB Interface(VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - Serial Peripheral Interface(SPI Interface)
  - VSYNC Interface
- Display Features
  - Programmable Partial Display Duty
  - Resizing Function (x1/2, x1/4)
- Support LC Type Option
  - MVA LC Type
  - Transflective LC Type
  - Transmissive LC Type
- On Chip Build-In Circuits
  - DC/DC Converter
  - Adjustable VCOM Generation
  - Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
  - Oscillator for Display Clock Generation
  - Timing Controller
- Build-In NV Memory for LCD Initial Register Setting
  - 7-bits for ID2
  - 5-bits for flicker adjustment

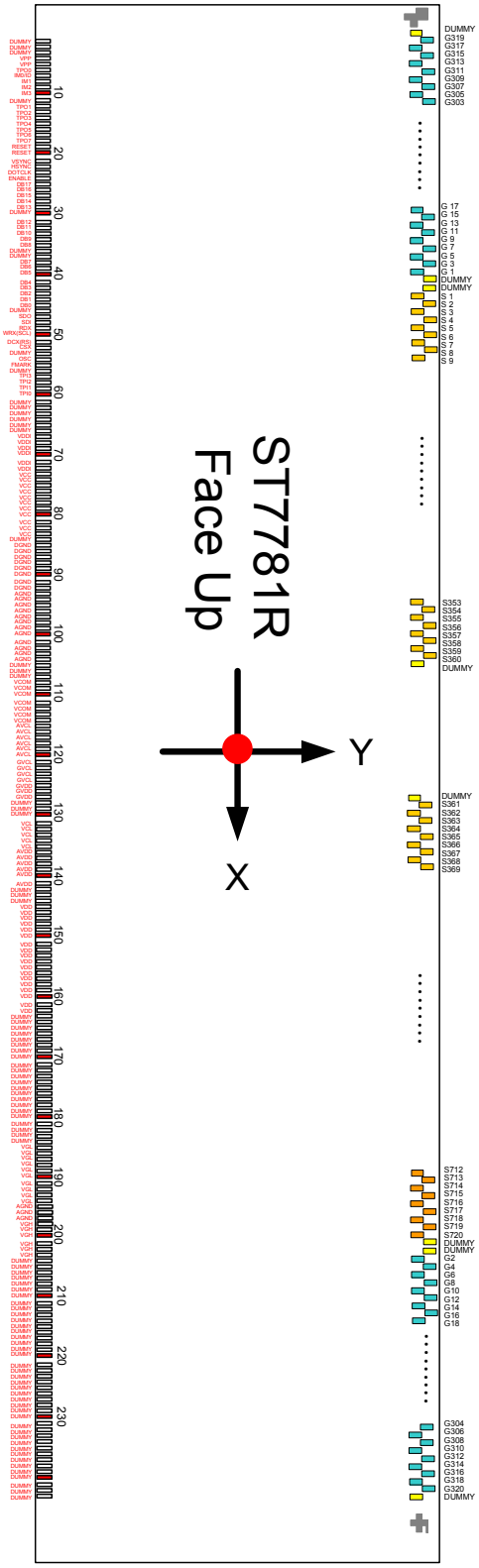
- Driving Algorithm
  - Dot Inversion
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V
  - Analog Voltage (VDD to AGND): 2.5V ~ 3.3V
- On-Chip Power System
  - Source Voltage (GVDD to GVCL): +4.7~-4.7V
  - VCOM level: -0.425V ~ -2V
  - Gate driver HIGH level (VGH to AGND): +10.0V ~ +15V
  - Gate driver LOW level (VGL to AGND): -13V ~ -7.5V
- Optimized layout for COG Assembly
- Operate temperature range: −30℃ to +85℃
- Lower Power Consumption

3 PAD ARRANGEMENT

3.1.. Output Bump Dimension

Au bump height	12μm
Au bump size	16μmx90μm Gate : G1~G320 Source : S1~S720
	50μmx80μm Input Pads : Pad1 to Pad243



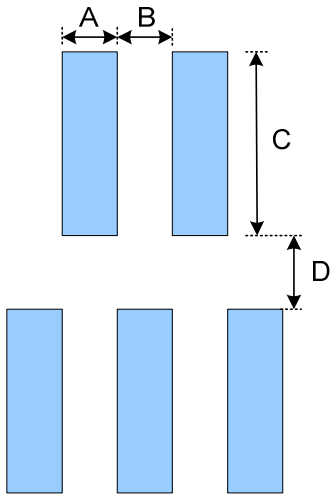


3.2.. Input Bump Dimension

- **Input Pads**

  S1~S720、G1~G320、DUMMY

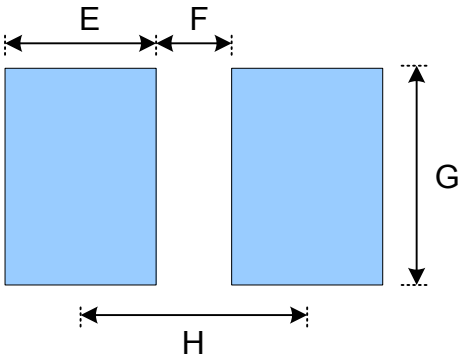
  (No.244~1291)



Symbol	Item	Size
A	Bump Width	16 um
B	Bump Gap 1 (Horizontal)	16 um
C	Bump Height	90 um
D	Bump Gap 2 (Vertical)	27 um

- **Output Pads**

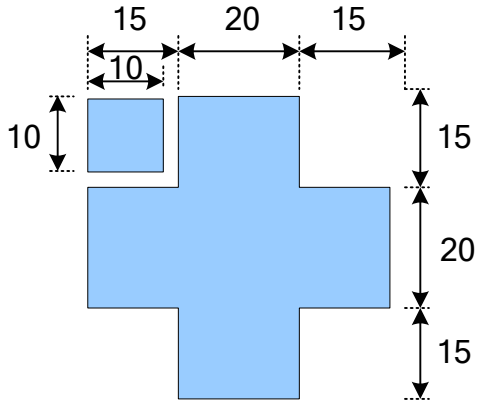
  No.1~243



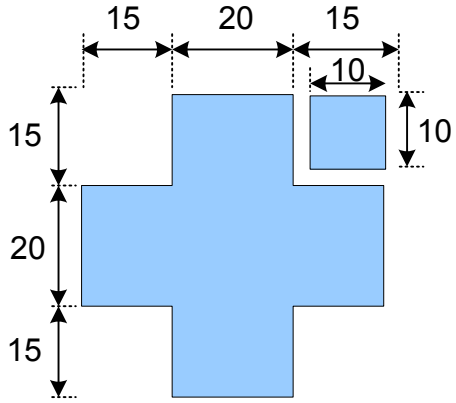
Symbol	Item	Size
E	Bump Width	50 um
F	Bump Gap	20、30、35 um
G	Bump Height	80 um
H	Bump Pitch	70、80、85 um

3.3.. Alignment Mark Dimension

- **Alignment Mark: A1(X,Y)=(8751,227.5)**



- **Alignment Mark: A2(X,Y)=(-8751,227.5)**



3.4.. Chip Information

Chip size	17688μm x750μm
Chip thickness	300μm
Pad Location	Pad center
Coordinate Origin	Chip center

4 PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DUMMY	-8610	-279	**34**	DB9	-6165	-279
2	DUMMY	-8540	-279	**35**	DB8	-6085	-279
3	DUMMY	-8470	-279	**36**	DUMMY	-5990	-279
4	VPP	-8400	-279	**37**	DUMMY	-5920	-279
5	VPP	-8330	-279	**38**	DB7	-5825	-279
6	TPO0	-8260	-279	**39**	DB6	-5745	-279
7	IM0/ID	-8190	-279	**40**	DB5	-5665	-279
8	IM1	-8120	-279	**41**	DB4	-5585	-279
9	IM2	-8050	-279	**42**	DB3	-5505	-279
10	IM3	-7980	-279	**43**	DB2	-5425	-279
11	DUMMY	-7910	-279	**44**	DB1	-5345	-279
12	TPO1	-7840	-279	**45**	DB0	-5265	-279
13	TPO2	-7770	-279	**46**	DUMMY	-5180	-279
14	TPO3	-7700	-279	**47**	SDO	-5110	-279
15	TPO4	-7630	-279	**48**	SDI	-5040	-279
16	TPO5	-7560	-279	**49**	RDX	-4970	-279
17	TPO6	-7490	-279	**50**	WRX(SCL)	-4900	-279
18	TPO7	-7420	-279	**51**	DCX(RS)	-4830	-279
19	RESET	-7350	-279	**52**	CSX	-4760	-279
20	RESET	-7280	-279	**53**	DUMMY	-4690	-279
21	VSYNC	-7210	-279	**54**	OSC	-4620	-279
22	HSYNC	-7140	-279	**55**	FMARK	-4550	-279
23	DOTCLK	-7070	-279	**56**	DUMMY	-4480	-279
24	ENABLE	-7000	-279	**57**	TPI3	-4410	-279
25	DB17	-6905	-279	**58**	TPI2	-4340	-279
26	DB16	-6825	-279	**59**	TPI1	-4270	-279
27	DB15	-6745	-279	**60**	TPI0	-4200	-279
28	DB14	-6665	-279	**61**	DUMMY	-4130	-279
29	DB13	-6585	-279	**62**	DUMMY	-4060	-279
30	DUMMY	-6495	-279	**63**	DUMMY	-3990	-279
31	DB12	-6405	-279	**64**	DUMMY	-3920	-279
32	DB11	-6325	-279	**65**	DUMMY	-3850	-279
33	DB10	-6245	-279	**66**	DUMMY	-3780	-279

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	VDDI	-3710	-279	**101**	AGND	-1330	-279
68	VDDI	-3640	-279	**102**	AGND	-1260	-279
69	VDDI	-3570	-279	**103**	AGND	-1190	-279
70	VDDI	-3500	-279	**104**	AGND	-1120	-279
71	VDDI	-3430	-279	**105**	DUMMY	-1050	-279
72	VDDI	-3360	-279	**106**	DUMMY	-980	-279
73	VCC	-3290	-279	**107**	DUMMY	-910	-279
74	VCC	-3220	-279	**108**	VCOM	-840	-279
75	VCC	-3150	-279	**109**	VCOM	-770	-279
76	VCC	-3080	-279	**110**	VCOM	-700	-279
77	VCC	-3010	-279	**111**	VCOM	-630	-279
78	VCC	-2940	-279	**112**	VCOM	-560	-279
79	VCC	-2870	-279	**113**	VCOM	-490	-279
80	VCC	-2800	-279	**114**	VCOM	-420	-279
81	VCC	-2730	-279	**115**	AVCL	-350	-279
82	VCC	-2660	-279	**116**	AVCL	-280	-279
83	VCC	-2590	-279	**117**	AVCL	-210	-279
84	DUMMY	-2520	-279	**118**	AVCL	-140	-279
85	DGND	-2450	-279	**119**	AVCL	-70	-279
86	DGND	-2380	-279	**120**	AVCL	0	-279
87	DGND	-2310	-279	**121**	GVCL	70	-279
88	DGND	-2240	-279	**122**	GVCL	140	-279
89	DGND	-2170	-279	**123**	GVCL	210	-279
90	DGND	-2100	-279	**124**	GVCL	280	-279
91	DGND	-2030	-279	**125**	GVDD	350	-279
92	DGND	-1960	-279	**126**	GVDD	420	-279
93	AGND	-1890	-279	**127**	GVDD	490	-279
94	AGND	-1820	-279	**128**	DUMMY	560	-279
95	AGND	-1750	-279	**129**	DUMMY	630	-279
96	AGND	-1680	-279	**130**	DUMMY	700	-279
97	AGND	-1610	-279	**131**	VCL	770	-279
98	AGND	-1540	-279	**132**	VCL	840	-279
99	AGND	-1470	-279	**133**	VCL	910	-279
100	AGND	-1400	-279	**134**	VCL	980	-279

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
135	VCL	1050	-279	**169**	DUMMY	3430	-279
136	AVDD	1120	-279	**170**	DUMMY	3500	-279
137	AVDD	1190	-279	**171**	DUMMY	3570	-279
138	AVDD	1260	-279	**172**	DUMMY	3640	-279
139	AVDD	1330	-279	**173**	DUMMY	3710	-279
140	AVDD	1400	-279	**174**	DUMMY	3780	-279
141	AVDD	1470	-279	**175**	DUMMY	3850	-279
142	DUMMY	1540	-279	**176**	DUMMY	3920	-279
143	DUMMY	1610	-279	**177**	DUMMY	3990	-279
144	DUMMY	1680	-279	**178**	DUMMY	4060	-279
145	VDD	1750	-279	**179**	DUMMY	4130	-279
146	VDD	1820	-279	**180**	DUMMY	4200	-279
147	VDD	1890	-279	**181**	DUMMY	4270	-279
148	VDD	1960	-279	**182**	DUMMY	4340	-279
149	VDD	2030	-279	**183**	DUMMY	4410	-279
150	VDD	2100	-279	**184**	DUMMY	4480	-279
151	VDD	2170	-279	**185**	VGL	4550	-279
152	VDD	2240	-279	**186**	VGL	4620	-279
153	VDD	2310	-279	**187**	VGL	4690	-279
154	VDD	2380	-279	**188**	VGL	4760	-279
155	VDD	2450	-279	**189**	VGL	4830	-279
156	VDD	2520	-279	**190**	VGL	4900	-279
157	VDD	2590	-279	**191**	VGL	4970	-279
158	VDD	2660	-279	**192**	VGL	5040	-279
159	VDD	2730	-279	**193**	VGL	5110	-279
160	VDD	2800	-279	**194**	VGL	5180	-279
161	VDD	2870	-279	**195**	AGND	5250	-279
162	VDD	2940	-279	**196**	AGND	5320	-279
163	DUMMY	3010	-279	**197**	AGND	5390	-279
164	DUMMY	3080	-279	**198**	VGH	5460	-279
165	DUMMY	3150	-279	**199**	VGH	5530	-279
166	DUMMY	3220	-279	**200**	VGH	5600	-279
167	DUMMY	3290	-279	**201**	VGH	5670	-279
168	DUMMY	3360	-279	**202**	VGH	5740	-279

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
203	VGH	5810	-279	**237**	DUMMY	8190	-279
204	DUMMY	5880	-279	**238**	DUMMY	8260	-279
205	DUMMY	5950	-279	**239**	DUMMY	8330	-279
206	DUMMY	6020	-279	**240**	DUMMY	8400	-279
207	DUMMY	6090	-279	**241**	DUMMY	8470	-279
208	DUMMY	6160	-279	**242**	DUMMY	8540	-279
209	DUMMY	6230	-279	**243**	DUMMY	8610	-279
210	DUMMY	6300	-279	**244**	DUMMY	8659	157
211	DUMMY	6370	-279	**245**	G320	8643	274
212	DUMMY	6440	-279	**246**	G318	8627	157
213	DUMMY	6510	-279	**247**	G316	8611	274
214	DUMMY	6580	-279	**248**	G314	8595	157
215	DUMMY	6650	-279	**249**	G312	8579	274
216	DUMMY	6720	-279	**250**	G310	8563	157
217	DUMMY	6790	-279	**251**	G308	8547	274
218	DUMMY	6860	-279	**252**	G306	8531	157
219	DUMMY	6930	-279	**253**	G304	8515	274
220	DUMMY	7000	-279	**254**	G302	8499	157
221	DUMMY	7070	-279	**255**	G300	8483	274
222	DUMMY	7140	-279	**256**	G298	8467	157
223	DUMMY	7210	-279	**257**	G296	8451	274
224	DUMMY	7280	-279	**258**	G294	8435	157
225	DUMMY	7350	-279	**259**	G292	8419	274
226	DUMMY	7420	-279	**260**	G290	8403	157
227	DUMMY	7490	-279	**261**	G288	8387	274
228	DUMMY	7560	-279	**262**	G286	8371	157
229	DUMMY	7630	-279	**263**	G284	8355	274
230	DUMMY	7700	-279	**264**	G282	8339	157
231	DUMMY	7770	-279	**265**	G280	8323	274
232	DUMMY	7840	-279	**266**	G278	8307	157
233	DUMMY	7910	-279	**267**	G276	8291	274
234	DUMMY	7980	-279	**268**	G274	8275	157
235	DUMMY	8050	-279	**269**	G272	8259	274
236	DUMMY	8120	-279	**270**	G270	8243	157

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
271	G268	8227	274	**305**	G200	7683	274
272	G266	8211	157	**306**	G198	7667	157
273	G264	8195	274	**307**	G196	7651	274
274	G262	8179	157	**308**	G194	7635	157
275	G260	8163	274	**309**	G192	7619	274
276	G258	8147	157	**310**	G190	7603	157
277	G256	8131	274	**311**	G188	7587	274
278	G254	8115	157	**312**	G186	7571	157
279	G252	8099	274	**313**	G184	7555	274
280	G250	8083	157	**314**	G182	7539	157
281	G248	8067	274	**315**	G180	7523	274
282	G246	8051	157	**316**	G178	7507	157
283	G244	8035	274	**317**	G176	7491	274
284	G242	8019	157	**318**	G174	7475	157
285	G240	8003	274	**319**	G172	7459	274
286	G238	7987	157	**320**	G170	7443	157
287	G236	7971	274	**321**	G168	7427	274
288	G234	7955	157	**322**	G166	7411	157
289	G232	7939	274	**323**	G164	7395	274
290	G230	7923	157	**324**	G162	7379	157
291	G228	7907	274	**325**	G160	7363	274
292	G226	7891	157	**326**	G158	7347	157
293	G224	7875	274	**327**	G156	7331	274
294	G222	7859	157	**328**	G154	7315	157
295	G220	7843	274	**329**	G152	7299	274
296	G218	7827	157	**330**	G150	7283	157
297	G216	7811	274	**331**	G148	7267	274
298	G214	7795	157	**332**	G146	7251	157
299	G212	7779	274	**333**	G144	7235	274
300	G210	7763	157	**334**	G142	7219	157
301	G208	7747	274	**335**	G140	7203	274
302	G206	7731	157	**336**	G138	7187	157
303	G204	7715	274	**337**	G136	7171	274
304	G202	7699	157	**338**	G134	7155	157

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
339	G132	7139	274	**373**	G64	6595	274
340	G130	7123	157	**374**	G62	6579	157
341	G128	7107	274	**375**	G60	6563	274
342	G126	7091	157	**376**	G58	6547	157
343	G124	7075	274	**377**	G56	6531	274
344	G122	7059	157	**378**	G54	6515	157
345	G120	7043	274	**379**	G52	6499	274
346	G118	7027	157	**380**	G50	6483	157
347	G116	7011	274	**381**	G48	6467	274
348	G114	6995	157	**382**	G46	6451	157
349	G112	6979	274	**383**	G44	6435	274
350	G110	6963	157	**384**	G42	6419	157
351	G108	6947	274	**385**	G40	6403	274
352	G106	6931	157	**386**	G38	6387	157
353	G104	6915	274	**387**	G36	6371	274
354	G102	6899	157	**388**	G34	6355	157
355	G100	6883	274	**389**	G32	6339	274
356	G98	6867	157	**390**	G30	6323	157
357	G96	6851	274	**391**	G28	6307	274
358	G94	6835	157	**392**	G26	6291	157
359	G92	6819	274	**393**	G24	6275	274
360	G90	6803	157	**394**	G22	6259	157
361	G88	6787	274	**395**	G20	6243	274
362	G86	6771	157	**396**	G18	6227	157
363	G84	6755	274	**397**	G16	6211	274
364	G82	6739	157	**398**	G14	6195	157
365	G80	6723	274	**399**	G12	6179	274
366	G78	6707	157	**400**	G10	6163	157
367	G76	6691	274	**401**	G8	6147	274
368	G74	6675	157	**402**	G6	6131	157
369	G72	6659	274	**403**	G4	6115	274
370	G70	6643	157	**404**	G2	6099	157
371	G68	6627	274	**405**	DUMMY	6083	274
372	G66	6611	157	**406**	DUMMY	6047	274

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
407	S720	6031	157	**441**	S686	5487	157
408	S719	6015	274	**442**	S685	5471	274
409	S718	5999	157	**443**	S684	5455	157
410	S717	5983	274	**444**	S683	5439	274
411	S716	5967	157	**445**	S682	5423	157
412	S715	5951	274	**446**	S681	5407	274
413	S714	5935	157	**447**	S680	5391	157
414	S713	5919	274	**448**	S679	5375	274
415	S712	5903	157	**449**	S678	5359	157
416	S711	5887	274	**450**	S677	5343	274
417	S710	5871	157	**451**	S676	5327	157
418	S709	5855	274	**452**	S675	5311	274
419	S708	5839	157	**453**	S674	5295	157
420	S707	5823	274	**454**	S673	5279	274
421	S706	5807	157	**455**	S672	5263	157
422	S705	5791	274	**456**	S671	5247	274
423	S704	5775	157	**457**	S670	5231	157
424	S703	5759	274	**458**	S669	5215	274
425	S702	5743	157	**459**	S668	5199	157
426	S701	5727	274	**460**	S667	5183	274
427	S700	5711	157	**461**	S666	5167	157
428	S699	5695	274	**462**	S665	5151	274
429	S698	5679	157	**463**	S664	5135	157
430	S697	5663	274	**464**	S663	5119	274
431	S696	5647	157	**465**	S662	5103	157
432	S695	5631	274	**466**	S661	5087	274
433	S694	5615	157	**467**	S660	5071	157
434	S693	5599	274	**468**	S659	5055	274
435	S692	5583	157	**469**	S658	5039	157
436	S691	5567	274	**470**	S657	5023	274
437	S690	5551	157	**471**	S656	5007	157
438	S689	5535	274	**472**	S655	4991	274
439	S688	5519	157	**473**	S654	4975	157
440	S687	5503	274	**474**	S653	4959	274

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
475	S652	4943	157	**509**	S618	4399	157
476	S651	4927	274	**510**	S617	4383	274
477	S650	4911	157	**511**	S616	4367	157
478	S649	4895	274	**512**	S615	4351	274
479	S648	4879	157	**513**	S614	4335	157
480	S647	4863	274	**514**	S613	4319	274
481	S646	4847	157	**515**	S612	4303	157
482	S645	4831	274	**516**	S611	4287	274
483	S644	4815	157	**517**	S610	4271	157
484	S643	4799	274	**518**	S609	4255	274
485	S642	4783	157	**519**	S608	4239	157
486	S641	4767	274	**520**	S607	4223	274
487	S640	4751	157	**521**	S606	4207	157
488	S639	4735	274	**522**	S605	4191	274
489	S638	4719	157	**523**	S604	4175	157
490	S637	4703	274	**524**	S603	4159	274
491	S636	4687	157	**525**	S602	4143	157
492	S635	4671	274	**526**	S601	4127	274
493	S634	4655	157	**527**	S600	4111	157
494	S633	4639	274	**528**	S599	4095	274
495	S632	4623	157	**529**	S598	4079	157
496	S631	4607	274	**530**	S597	4063	274
497	S630	4591	157	**531**	S596	4047	157
498	S629	4575	274	**532**	S595	4031	274
499	S628	4559	157	**533**	S594	4015	157
500	S627	4543	274	**534**	S593	3999	274
501	S626	4527	157	**535**	S592	3983	157
502	S625	4511	274	**536**	S591	3967	274
503	S624	4495	157	**537**	S590	3951	157
504	S623	4479	274	**538**	S589	3935	274
505	S622	4463	157	**539**	S588	3919	157
506	S621	4447	274	**540**	S587	3903	274
507	S620	4431	157	**541**	S586	3887	157
508	S619	4415	274	**542**	S585	3871	274

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
543	S584	3855	157	**577**	S550	3311	157
544	S583	3839	274	**578**	S549	3295	274
545	S582	3823	157	**579**	S548	3279	157
546	S581	3807	274	**580**	S547	3263	274
547	S580	3791	157	**581**	S546	3247	157
548	S579	3775	274	**582**	S545	3231	274
549	S578	3759	157	**583**	S544	3215	157
550	S577	3743	274	**584**	S543	3199	274
551	S576	3727	157	**585**	S542	3183	157
552	S575	3711	274	**586**	S541	3167	274
553	S574	3695	157	**587**	S540	3151	157
554	S573	3679	274	**588**	S539	3135	274
555	S572	3663	157	**589**	S538	3119	157
556	S571	3647	274	**590**	S537	3103	274
557	S570	3631	157	**591**	S536	3087	157
558	S569	3615	274	**592**	S535	3071	274
559	S568	3599	157	**593**	S534	3055	157
560	S567	3583	274	**594**	S533	3039	274
561	S566	3567	157	**595**	S532	3023	157
562	S565	3551	274	**596**	S531	3007	274
563	S564	3535	157	**597**	S530	2991	157
564	S563	3519	274	**598**	S529	2975	274
565	S562	3503	157	**599**	S528	2959	157
566	S561	3487	274	**600**	S527	2943	274
567	S560	3471	157	**601**	S526	2927	157
568	S559	3455	274	**602**	S525	2911	274
569	S558	3439	157	**603**	S524	2895	157
570	S557	3423	274	**604**	S523	2879	274
571	S556	3407	157	**605**	S522	2863	157
572	S555	3391	274	**606**	S521	2847	274
573	S554	3375	157	**607**	S520	2831	157
574	S553	3359	274	**608**	S519	2815	274
575	S552	3343	157	**609**	S518	2799	157
576	S551	3327	274	**610**	S517	2783	274

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
611	S516	2767	157	**645**	S482	2223	157
612	S515	2751	274	**646**	S481	2207	274
613	S514	2735	157	**647**	S480	2191	157
614	S513	2719	274	**648**	S479	2175	274
615	S512	2703	157	**649**	S478	2159	157
616	S511	2687	274	**650**	S477	2143	274
617	S510	2671	157	**651**	S476	2127	157
618	S509	2655	274	**652**	S475	2111	274
619	S508	2639	157	**653**	S474	2095	157
620	S507	2623	274	**654**	S473	2079	274
621	S506	2607	157	**655**	S472	2063	157
622	S505	2591	274	**656**	S471	2047	274
623	S504	2575	157	**657**	S470	2031	157
624	S503	2559	274	**658**	S469	2015	274
625	S502	2543	157	**659**	S468	1999	157
626	S501	2527	274	**660**	S467	1983	274
627	S500	2511	157	**661**	S466	1967	157
628	S499	2495	274	**662**	S465	1951	274
629	S498	2479	157	**663**	S464	1935	157
630	S497	2463	274	**664**	S463	1919	274
631	S496	2447	157	**665**	S462	1903	157
632	S495	2431	274	**666**	S461	1887	274
633	S494	2415	157	**667**	S460	1871	157
634	S493	2399	274	**668**	S459	1855	274
635	S492	2383	157	**669**	S458	1839	157
636	S491	2367	274	**670**	S457	1823	274
637	S490	2351	157	**671**	S456	1807	157
638	S489	2335	274	**672**	S455	1791	274
639	S488	2319	157	**673**	S454	1775	157
640	S487	2303	274	**674**	S453	1759	274
641	S486	2287	157	**675**	S452	1743	157
642	S485	2271	274	**676**	S451	1727	274
643	S484	2255	157	**677**	S450	1711	157
644	S483	2239	274	**678**	S449	1695	274

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
679	S448	1679	157	**713**	S414	1135	157
680	S447	1663	274	**714**	S413	1119	274
681	S446	1647	157	**715**	S412	1103	157
682	S445	1631	274	**716**	S411	1087	274
683	S444	1615	157	**717**	S410	1071	157
684	S443	1599	274	**718**	S409	1055	274
685	S442	1583	157	**719**	S408	1039	157
686	S441	1567	274	**720**	S407	1023	274
687	S440	1551	157	**721**	S406	1007	157
688	S439	1535	274	**722**	S405	991	274
689	S438	1519	157	**723**	S404	975	157
690	S437	1503	274	**724**	S403	959	274
691	S436	1487	157	**725**	S402	943	157
692	S435	1471	274	**726**	S401	927	274
693	S434	1455	157	**727**	S400	911	157
694	S433	1439	274	**728**	S399	895	274
695	S432	1423	157	**729**	S398	879	157
696	S431	1407	274	**730**	S397	863	274
697	S430	1391	157	**731**	S396	847	157
698	S429	1375	274	**732**	S395	831	274
699	S428	1359	157	**733**	S394	815	157
700	S427	1343	274	**734**	S393	799	274
701	S426	1327	157	**735**	S392	783	157
702	S425	1311	274	**736**	S391	767	274
703	S424	1295	157	**737**	S390	751	157
704	S423	1279	274	**738**	S389	735	274
705	S422	1263	157	**739**	S388	719	157
706	S421	1247	274	**740**	S387	703	274
707	S420	1231	157	**741**	S386	687	157
708	S419	1215	274	**742**	S385	671	274
709	S418	1199	157	**743**	S384	655	157
710	S417	1183	274	**744**	S383	639	274
711	S416	1167	157	**745**	S382	623	157
712	S415	1151	274	**746**	S381	607	274

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
747	S380	591	157	**781**	S348	-479	274
748	S379	575	274	**782**	S347	-495	157
749	S378	559	157	**783**	S346	-511	274
750	S377	543	274	**784**	S345	-527	157
751	S376	527	157	**785**	S344	-543	274
752	S375	511	274	**786**	S343	-559	157
753	S374	495	157	**787**	S342	-575	274
754	S373	479	274	**788**	S341	-591	157
755	S372	463	157	**789**	S340	-607	274
756	S371	447	274	**790**	S339	-623	157
757	S370	431	157	**791**	S338	-639	274
758	S369	415	274	**792**	S337	-655	157
759	S368	399	157	**793**	S336	-671	274
760	S367	383	274	**794**	S335	-687	157
761	S366	367	157	**795**	S334	-703	274
762	S365	351	274	**796**	S333	-719	157
763	S364	335	157	**797**	S332	-735	274
764	S363	319	274	**798**	S331	-751	157
765	S362	303	157	**799**	S330	-767	274
766	S361	287	274	**800**	S329	-783	157
767	DUMMY	271	157	**801**	S328	-799	274
768	DUMMY	-271	157	**802**	S327	-815	157
769	S360	-287	274	**803**	S326	-831	274
770	S359	-303	157	**804**	S325	-847	157
771	S358	-319	274	**805**	S324	-863	274
772	S357	-335	157	**806**	S323	-879	157
773	S356	-351	274	**807**	S322	-895	274
774	S355	-367	157	**808**	S321	-911	157
775	S354	-383	274	**809**	S320	-927	274
776	S353	-399	157	**810**	S319	-943	157
777	S352	-415	274	**811**	S318	-959	274
778	S351	-431	157	**812**	S317	-975	157
779	S350	-447	274	**813**	S316	-991	274
780	S349	-463	157	**814**	S315	-1007	157

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
815	S314	-1023	274	**849**	S280	-1567	274
816	S313	-1039	157	**850**	S279	-1583	157
817	S312	-1055	274	**851**	S278	-1599	274
818	S311	-1071	157	**852**	S277	-1615	157
819	S310	-1087	274	**853**	S276	-1631	274
820	S309	-1103	157	**854**	S275	-1647	157
821	S308	-1119	274	**855**	S274	-1663	274
822	S307	-1135	157	**856**	S273	-1679	157
823	S306	-1151	274	**857**	S272	-1695	274
824	S305	-1167	157	**858**	S271	-1711	157
825	S304	-1183	274	**859**	S270	-1727	274
826	S303	-1199	157	**860**	S269	-1743	157
827	S302	-1215	274	**861**	S268	-1759	274
828	S301	-1231	157	**862**	S267	-1775	157
829	S300	-1247	274	**863**	S266	-1791	274
830	S299	-1263	157	**864**	S265	-1807	157
831	S298	-1279	274	**865**	S264	-1823	274
832	S297	-1295	157	**866**	S263	-1839	157
833	S296	-1311	274	**867**	S262	-1855	274
834	S295	-1327	157	**868**	S261	-1871	157
835	S294	-1343	274	**869**	S260	-1887	274
836	S293	-1359	157	**870**	S259	-1903	157
837	S292	-1375	274	**871**	S258	-1919	274
838	S291	-1391	157	**872**	S257	-1935	157
839	S290	-1407	274	**873**	S256	-1951	274
840	S289	-1423	157	**874**	S255	-1967	157
841	S288	-1439	274	**875**	S254	-1983	274
842	S287	-1455	157	**876**	S253	-1999	157
843	S286	-1471	274	**877**	S252	-2015	274
844	S285	-1487	157	**878**	S251	-2031	157
845	S284	-1503	274	**879**	S250	-2047	274
846	S283	-1519	157	**880**	S249	-2063	157
847	S282	-1535	274	**881**	S248	-2079	274
848	S281	-1551	157	**882**	S247	-2095	157

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
883	S246	-2111	274	**917**	S212	-2655	274
884	S245	-2127	157	**918**	S211	-2671	157
885	S244	-2143	274	**919**	S210	-2687	274
886	S243	-2159	157	**920**	S209	-2703	157
887	S242	-2175	274	**921**	S208	-2719	274
888	S241	-2191	157	**922**	S207	-2735	157
889	S240	-2207	274	**923**	S206	-2751	274
890	S239	-2223	157	**924**	S205	-2767	157
891	S238	-2239	274	**925**	S204	-2783	274
892	S237	-2255	157	**926**	S203	-2799	157
893	S236	-2271	274	**927**	S202	-2815	274
894	S235	-2287	157	**928**	S201	-2831	157
895	S234	-2303	274	**929**	S200	-2847	274
896	S233	-2319	157	**930**	S199	-2863	157
897	S232	-2335	274	**931**	S198	-2879	274
898	S231	-2351	157	**932**	S197	-2895	157
899	S230	-2367	274	**933**	S196	-2911	274
900	S229	-2383	157	**934**	S195	-2927	157
901	S228	-2399	274	**935**	S194	-2943	274
902	S227	-2415	157	**936**	S193	-2959	157
903	S226	-2431	274	**937**	S192	-2975	274
904	S225	-2447	157	**938**	S191	-2991	157
905	S224	-2463	274	**939**	S190	-3007	274
906	S223	-2479	157	**940**	S189	-3023	157
907	S222	-2495	274	**941**	S188	-3039	274
908	S221	-2511	157	**942**	S187	-3055	157
909	S220	-2527	274	**943**	S186	-3071	274
910	S219	-2543	157	**944**	S185	-3087	157
911	S218	-2559	274	**945**	S184	-3103	274
912	S217	-2575	157	**946**	S183	-3119	157
913	S216	-2591	274	**947**	S182	-3135	274
914	S215	-2607	157	**948**	S181	-3151	157
915	S214	-2623	274	**949**	S180	-3167	274
916	S213	-2639	157	**950**	S179	-3183	157

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
951	S178	-3199	274	**985**	S144	-3743	274
952	S177	-3215	157	**986**	S143	-3759	157
953	S176	-3231	274	**987**	S142	-3775	274
954	S175	-3247	157	**988**	S141	-3791	157
955	S174	-3263	274	**989**	S140	-3807	274
956	S173	-3279	157	**990**	S139	-3823	157
957	S172	-3295	274	**991**	S138	-3839	274
958	S171	-3311	157	**992**	S137	-3855	157
959	S170	-3327	274	**993**	S136	-3871	274
960	S169	-3343	157	**994**	S135	-3887	157
961	S168	-3359	274	**995**	S134	-3903	274
962	S167	-3375	157	**996**	S133	-3919	157
963	S166	-3391	274	**997**	S132	-3935	274
964	S165	-3407	157	**998**	S131	-3951	157
965	S164	-3423	274	**999**	S130	-3967	274
966	S163	-3439	157	**1000**	S129	-3983	157
967	S162	-3455	274	**1001**	S128	-3999	274
968	S161	-3471	157	**1002**	S127	-4015	157
969	S160	-3487	274	**1003**	S126	-4031	274
970	S159	-3503	157	**1004**	S125	-4047	157
971	S158	-3519	274	**1005**	S124	-4063	274
972	S157	-3535	157	**1006**	S123	-4079	157
973	S156	-3551	274	**1007**	S122	-4095	274
974	S155	-3567	157	**1008**	S121	-4111	157
975	S154	-3583	274	**1009**	S120	-4127	274
976	S153	-3599	157	**1010**	S119	-4143	157
977	S152	-3615	274	**1011**	S118	-4159	274
978	S151	-3631	157	**1012**	S117	-4175	157
979	S150	-3647	274	**1013**	S116	-4191	274
980	S149	-3663	157	**1014**	S115	-4207	157
981	S148	-3679	274	**1015**	S114	-4223	274
982	S147	-3695	157	**1016**	S113	-4239	157
983	S146	-3711	274	**1017**	S112	-4255	274
984	S145	-3727	157	**1018**	S111	-4271	157

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1019	S110	-4287	274	**1053**	S76	-4831	274
1020	S109	-4303	157	**1054**	S75	-4847	157
1021	S108	-4319	274	**1055**	S74	-4863	274
1022	S107	-4335	157	**1056**	S73	-4879	157
1023	S106	-4351	274	**1057**	S72	-4895	274
1024	S105	-4367	157	**1058**	S71	-4911	157
1025	S104	-4383	274	**1059**	S70	-4927	274
1026	S103	-4399	157	**1060**	S69	-4943	157
1027	S102	-4415	274	**1061**	S68	-4959	274
1028	S101	-4431	157	**1062**	S67	-4975	157
1029	S100	-4447	274	**1063**	S66	-4991	274
1030	S99	-4463	157	**1064**	S65	-5007	157
1031	S98	-4479	274	**1065**	S64	-5023	274
1032	S97	-4495	157	**1066**	S63	-5039	157
1033	S96	-4511	274	**1067**	S62	-5055	274
1034	S95	-4527	157	**1068**	S61	-5071	157
1035	S94	-4543	274	**1069**	S60	-5087	274
1036	S93	-4559	157	**1070**	S59	-5103	157
1037	S92	-4575	274	**1071**	S58	-5119	274
1038	S91	-4591	157	**1072**	S57	-5135	157
1039	S90	-4607	274	**1073**	S56	-5151	274
1040	S89	-4623	157	**1074**	S55	-5167	157
1041	S88	-4639	274	**1075**	S54	-5183	274
1042	S87	-4655	157	**1076**	S53	-5199	157
1043	S86	-4671	274	**1077**	S52	-5215	274
1044	S85	-4687	157	**1078**	S51	-5231	157
1045	S84	-4703	274	**1079**	S50	-5247	274
1046	S83	-4719	157	**1080**	S49	-5263	157
1047	S82	-4735	274	**1081**	S48	-5279	274
1048	S81	-4751	157	**1082**	S47	-5295	157
1049	S80	-4767	274	**1083**	S46	-5311	274
1050	S79	-4783	157	**1084**	S45	-5327	157
1051	S78	-4799	274	**1085**	S44	-5343	274
1052	S77	-4815	157	**1086**	S43	-5359	157

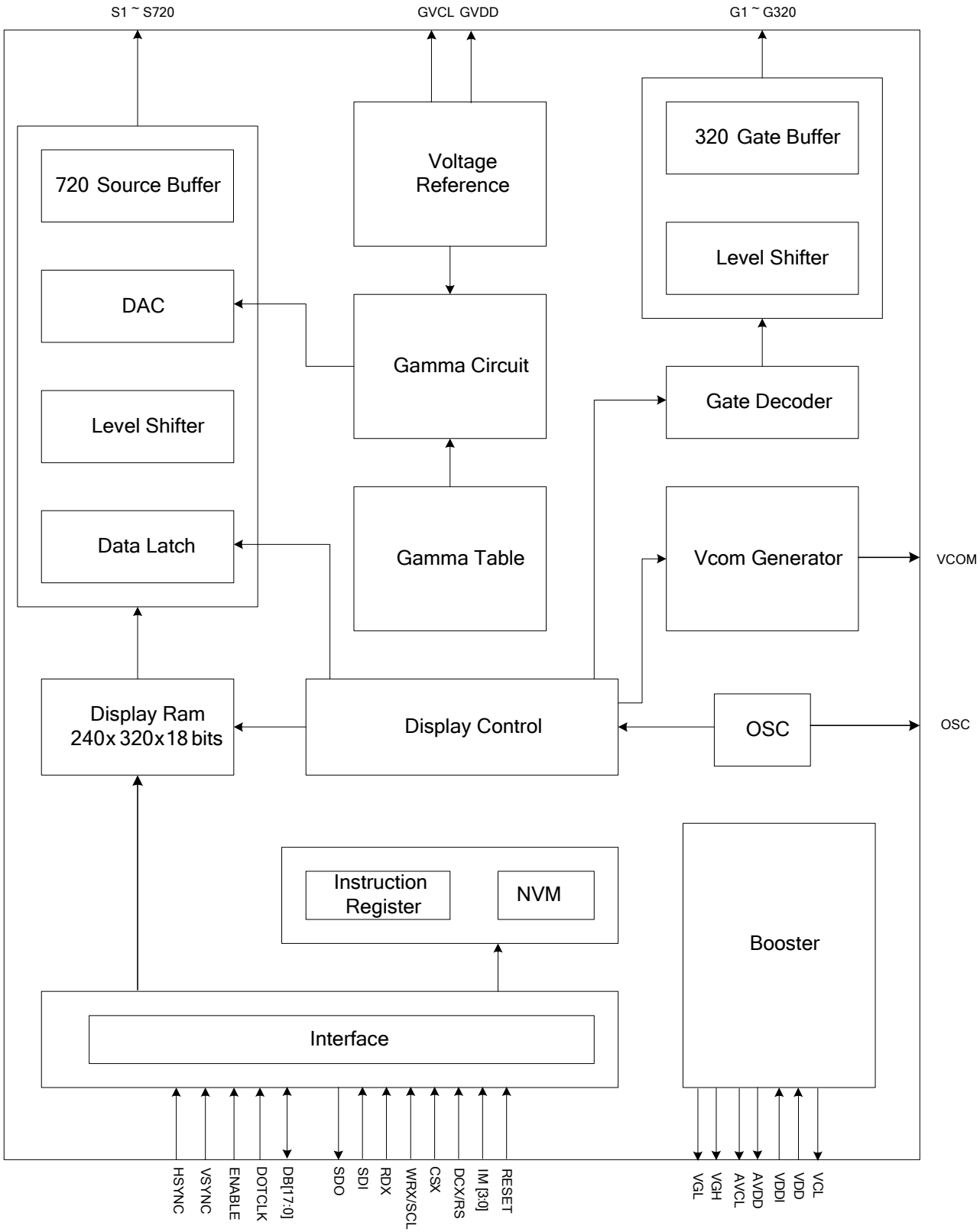
PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1087	S42	-5375	274	**1121**	S8	-5919	274
1088	S41	-5391	157	**1122**	S7	-5935	157
1089	S40	-5407	274	**1123**	S6	-5951	274
1090	S39	-5423	157	**1124**	S5	-5967	157
1091	S38	-5439	274	**1125**	S4	-5983	274
1092	S37	-5455	157	**1126**	S3	-5999	157
1093	S36	-5471	274	**1127**	S2	-6015	274
1094	S35	-5487	157	**1128**	S1	-6031	157
1095	S34	-5503	274	**1129**	DUMMY	-6047	274
1096	S33	-5519	157	**1130**	DUMMY	-6083	274
1097	S32	-5535	274	**1131**	G1	-6099	157
1098	S31	-5551	157	**1132**	G3	-6115	274
1099	S30	-5567	274	**1133**	G5	-6131	157
1100	S29	-5583	157	**1134**	G7	-6147	274
1101	S28	-5599	274	**1135**	G9	-6163	157
1102	S27	-5615	157	**1136**	G11	-6179	274
1103	S26	-5631	274	**1137**	G13	-6195	157
1104	S25	-5647	157	**1138**	G15	-6211	274
1105	S24	-5663	274	**1139**	G17	-6227	157
1106	S23	-5679	157	**1140**	G19	-6243	274
1107	S22	-5695	274	**1141**	G21	-6259	157
1108	S21	-5711	157	**1142**	G23	-6275	274
1109	S20	-5727	274	**1143**	G25	-6291	157
1110	S19	-5743	157	**1144**	G27	-6307	274
1111	S18	-5759	274	**1145**	G29	-6323	157
1112	S17	-5775	157	**1146**	G31	-6339	274
1113	S16	-5791	274	**1147**	G33	-6355	157
1114	S15	-5807	157	**1148**	G35	-6371	274
1115	S14	-5823	274	**1149**	G37	-6387	157
1116	S13	-5839	157	**1150**	G39	-6403	274
1117	S12	-5855	274	**1151**	G41	-6419	157
1118	S11	-5871	157	**1152**	G43	-6435	274
1119	S10	-5887	274	**1153**	G45	-6451	157
1120	S9	-5903	157	**1154**	G47	-6467	274

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1155	G49	-6483	157	**1189**	G117	-7027	157
1156	G51	-6499	274	**1190**	G119	-7043	274
1157	G53	-6515	157	**1191**	G121	-7059	157
1158	G55	-6531	274	**1192**	G123	-7075	274
1159	G57	-6547	157	**1193**	G125	-7091	157
1160	G59	-6563	274	**1194**	G127	-7107	274
1161	G61	-6579	157	**1195**	G129	-7123	157
1162	G63	-6595	274	**1196**	G131	-7139	274
1163	G65	-6611	157	**1197**	G133	-7155	157
1164	G67	-6627	274	**1198**	G135	-7171	274
1165	G69	-6643	157	**1199**	G137	-7187	157
1166	G71	-6659	274	**1200**	G139	-7203	274
1167	G73	-6675	157	**1201**	G141	-7219	157
1168	G75	-6691	274	**1202**	G143	-7235	274
1169	G77	-6707	157	**1203**	G145	-7251	157
1170	G79	-6723	274	**1204**	G147	-7267	274
1171	G81	-6739	157	**1205**	G149	-7283	157
1172	G83	-6755	274	**1206**	G151	-7299	274
1173	G85	-6771	157	**1207**	G153	-7315	157
1174	G87	-6787	274	**1208**	G155	-7331	274
1175	G89	-6803	157	**1209**	G157	-7347	157
1176	G91	-6819	274	**1210**	G159	-7363	274
1177	G93	-6835	157	**1211**	G161	-7379	157
1178	G95	-6851	274	**1212**	G163	-7395	274
1179	G97	-6867	157	**1213**	G165	-7411	157
1180	G99	-6883	274	**1214**	G167	-7427	274
1181	G101	-6899	157	**1215**	G169	-7443	157
1182	G103	-6915	274	**1216**	G171	-7459	274
1183	G105	-6931	157	**1217**	G173	-7475	157
1184	G107	-6947	274	**1218**	G175	-7491	274
1185	G109	-6963	157	**1219**	G177	-7507	157
1186	G111	-6979	274	**1220**	G179	-7523	274
1187	G113	-6995	157	**1221**	G181	-7539	157
1188	G115	-7011	274	**1222**	G183	-7555	274

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1223	G185	-7571	157	**1257**	G253	-8115	157
1224	G187	-7587	274	**1258**	G255	-8131	274
1225	G189	-7603	157	**1259**	G257	-8147	157
1226	G191	-7619	274	**1260**	G259	-8163	274
1227	G193	-7635	157	**1261**	G261	-8179	157
1228	G195	-7651	274	**1262**	G263	-8195	274
1229	G197	-7667	157	**1263**	G265	-8211	157
1230	G199	-7683	274	**1264**	G267	-8227	274
1231	G201	-7699	157	**1265**	G269	-8243	157
1232	G203	-7715	274	**1266**	G271	-8259	274
1233	G205	-7731	157	**1267**	G273	-8275	157
1234	G207	-7747	274	**1268**	G275	-8291	274
1235	G209	-7763	157	**1269**	G277	-8307	157
1236	G211	-7779	274	**1270**	G279	-8323	274
1237	G213	-7795	157	**1271**	G281	-8339	157
1238	G215	-7811	274	**1272**	G283	-8355	274
1239	G217	-7827	157	**1273**	G285	-8371	157
1240	G219	-7843	274	**1274**	G287	-8387	274
1241	G221	-7859	157	**1275**	G289	-8403	157
1242	G223	-7875	274	**1276**	G291	-8419	274
1243	G225	-7891	157	**1277**	G293	-8435	157
1244	G227	-7907	274	**1278**	G295	-8451	274
1245	G229	-7923	157	**1279**	G297	-8467	157
1246	G231	-7939	274	**1280**	G299	-8483	274
1247	G233	-7955	157	**1281**	G301	-8499	157
1248	G235	-7971	274	**1282**	G303	-8515	274
1249	G237	-7987	157	**1283**	G305	-8531	157
1250	G239	-8003	274	**1284**	G307	-8547	274
1251	G241	-8019	157	**1285**	G309	-8563	157
1252	G243	-8035	274	**1286**	G311	-8579	274
1253	G245	-8051	157	**1287**	G313	-8595	157
1254	G247	-8067	274	**1288**	G315	-8611	274
1255	G249	-8083	157	**1289**	G317	-8627	157
1256	G251	-8099	274	**1290**	G319	-8643	274

PAD No.	PIN Name	X	Y
1291	DUMMY	-8659	157

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1.. Power Supply Pins

Name	I/O	Description	Connect Pin
VDD	I	Power Supply for Analog, Digital System and Booster Circuit.	VDD
VDDI	I	Power Supply for I/O System.	VDDI
AGND	I	System Ground for Analog System and Booster Circuit.	GND
DGND	I	System Ground for I/O System and Digital System.	GND

6.2.. Interface Logic Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>IM3, IM2,
IM1, IM0/ID</td><td>I</td><td>-The MCU interface mode select.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-16bit</td><td>DB[17:10],
DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-8 bit</td><td>DB[17:10],</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>SPI</td><td>SDI, SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>--</td><td>Setting invalid</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-18bit</td><td>DB[17:0],</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-9bit</td><td>DB[17:9],</td></tr>
<tr><td>1</td><td>1</td><td>--</td><td>--</td><td>Setting invalid</td><td></td></tr>
</table>
-When the SPI interface is selected, IM0 pin will be used for the ID setting.</td><td>DGND/VDDI</td></tr>
<tr><td>RESET</td><td>I</td><td>-This signal will reset the device and it must be applied to properly initialize the chip.
-Signal is active low.</td><td>MCU</td></tr>
<tr><td>CSX</td><td>I</td><td>-Chip selection pin
Low enable.
High disable.</td><td>MCU</td></tr>
<tr><td>DCX
(RS)</td><td>I</td><td>-Display data/command selection pin in MCU interface.
DCX=’1’: display data or parameter.
DCX=’0’: command data.
-If not used, please fix this pin at VDDI or DGND level.</td><td>MCU</td></tr>
<tr><td>RDX</td><td>I</td><td>-Read enable in 8080 MCU parallel interface.
-If not used, please fix this pin at VDDI or DGND level.</td><td>MCU</td></tr>
<tr><td>WRX
(SCL)</td><td>I</td><td>-Write enable in MCU parallel interface.
In SPI mode, this is used as SCL.
-If not used, please fix this pin at VDDI or DGND level.</td><td>MCU</td></tr>
<tr><td>VSYNC</td><td>I</td><td>-Vertical (Frame) synchronizing input signal for RGB interface operation.
VSPL = “0”: Active low.
VSPL = “1”: Active high.</td><td>MCU</td></tr>
</table>

Name	I/O	Description	Connect Pin
		-Fix to the GND level when not in use.	
HSYNC	I	-Horizontal (Line) synchronizing input signal for RGB interface operation. HSPL = “0”: Active low. HSPL = “1”: Active high. -Fix to the GND level when not in use	MCU
ENABLE	I	-Data enable signal for RGB interface operation. Low: Select (access enabled) High: Not select (access disabled) The EPL bit inverts the polarity of the ENABLE signal. -If not used, please fix this pin at VDDI or DGND level.	MCU
DOTCLK	I	-Dot clock signal for RGB interface operation. DPL = “0”: Input data on the rising edge of DOTCLK DPL = “1”: Input data on the falling edge of DOTCLK -If not used, please fix this pin at DGND level.	MCU
SDI	I	-SPI interface input pin. -The data is latched on the rising edge of the SCL signal. -If not used, please fix this pin at VDDI or DGND level.	MCU
SDO	O	-SPI interface output pin. -The data is outputted on the falling edge of the SCL signal. If not used, please fix this pin at floating.	MCU
DB[17:0]	I/O	-DB[17:0] are used as MCU parallel interface data bus. 8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. -DB[17:0] are used as RGB interface data bus. 6-bit RGB I/F: DB[17:12] are used. 16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. -If not used, please fix this pin at VDDI or DGND level.	MCU
FMARK	O	-Output a frame head pulse signal is used as synchronies MCU to frame rate -If not used, Let this pin open	MCU

Note1. “1” = VDDI level, “0” = DGND level.

Note2. When in parallel mode, unused data pins must be connected to “1” or “0”.

Note3. When CSX=”1”, there is no influence to the parallel and serial interface.

6.3.. Driver Output Pins

Name	I/O	Description	Connect pin
S1 to S720	O	-Source driver output pins -To change the shift direction of signal outputs, use the SS bit. SS = “0”, the data in the RAM address “h00000” is output from S1. SS = “1”, the data in the RAM address “h00000” is output from S720. -When SS=”0” S1, S4, S7, … display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9 ... display blue (B)	LCD
G1 to G320	O	-Gate driver output pins. VGH: Selecting Gate Lines Level. VGL: Non-selecting Gate Lines Level.	LCD
AVDD	O	-Power pad for analogy circuit. -Connect a capacitor for stabilization.	Capacitor
GVDD	O	- A power output of grayscale voltage generator. - When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin.	-
AVCL	O	- A power supply pin for generating GVCL. - Connect a capacitor for stabilization.	Capacitor
GVCL	O	- A power output (Negative) of grayscale voltage generator. - When internal GVCL generator is not used, connect an external power supply (AVCL+0.5V) to this pin.	-
VCL	O	- A power output of VCOM voltage (Negative) generator.	-
VGH	O	- Power output pin for gate driver	-
VGL	O	- Power output (Negative) pin for gate driver	-
VCC	O	- Monitoring pin of internal digital reference voltage.	-
VCOM	O	- A power supply for the TFT-LCD common electrode.	Common Electrode
VPP	I	- When writing NVM, it needs external power supply voltage (7.5V). - If not used, Let this pin open.	

6.4.. Test Pins

Name	I/O	Description	Connect pin
TPI3 TPI2 TPI1 TPI0	I	-These test pins for Driver vender test used. -Please connect these pins to DGND.	DGND
TPO7 TPO6 TPO5 TPO4 TPO3 TPO2 TPO1 TPO0	O	-These test pins for Driver vender test used. -Please open these pins.	Open
OSC	O	-This pin is for testing. -Please let these pin open.	-
Dummy	-	-These pins are dummy (have no function inside). -Can allow signal traces pass through these pads on TFT glass. -Please open these pins.	Open

6.5.. Maximum allowable resistance

PAD No.	PIN Name	Resistance	PAD No.	PIN Name	Resistance	PAD No.	PIN Name	Resistance
1	DUMMY	Don't care	**34**	DB9	100Ω	**67**	VDDI	5Ω
2	DUMMY		**35**	DB8	100Ω	**68**	VDDI	
3	DUMMY		**36**	DUMMY	Don't care	**69**	VDDI	
4	VPP	5Ω	**37**	DUMMY		**70**	VDDI	
5	VPP		**38**	DB7	100Ω	**71**	VDDI	
6	TPO0	100Ω	**39**	DB6	100Ω	**72**	VDDI	
7	IM0/ID	100Ω	**40**	DB5	100Ω	**73**	VCC	50Ω
8	IM1	100Ω	**41**	DB4	100Ω	**74**	VCC	
9	IM2	100Ω	**42**	DB3	100Ω	**75**	VCC	
10	IM3	100Ω	**43**	DB2	100Ω	**76**	VCC	
11	DUMMY	Don't care	**44**	DB1	100Ω	**77**	VCC	
12	TPO1	100Ω	**45**	DB0	100Ω	**78**	VCC	
13	TPO2	100Ω	**46**	DUMMY	Don't care	**79**	VCC	
14	TPO3	100Ω	**47**	SDO	100Ω	**80**	VCC	
15	TPO4	100Ω	**48**	SDI	100Ω	**81**	VCC	
16	TPO5	100Ω	**49**	RDX	100Ω	**82**	VCC	
17	TPO6	100Ω	**50**	WRX(SCL)	100Ω	**83**	VCC	
18	TPO7	100Ω	**51**	DCX(RS)	100Ω	**84**	DUMMY	Don't care
19	RESET	100Ω	**52**	CSX	100Ω	**85**	DGND	5Ω
20	RESET	100Ω	**53**	DUMMY	Don't care	**86**	DGND	
21	VSYNC	100Ω	**54**	OSC	100Ω	**87**	DGND	
22	HSYNC	100Ω	**55**	FMARK	100Ω	**88**	DGND	
23	DOTCLK	100Ω	**56**	DUMMY	Don't care	**89**	DGND	
24	ENABLE	100Ω	**57**	TPI3	100Ω	**90**	DGND	
25	DB17	100Ω	**58**	TPI2	100Ω	**91**	DGND	
26	DB16	100Ω	**59**	TPI1	100Ω	**92**	DGND	
27	DB15	100Ω	**60**	TPI0	100Ω	**93**	AGND	5Ω
28	DB14	100Ω	**61**	DUMMY	Don't care	**94**	AGND	
29	DB13	100Ω	**62**	DUMMY		**95**	AGND	
30	DUMMY	Don't care	**63**	DUMMY		**96**	AGND	
31	DB12	100Ω	**64**	DUMMY		**97**	AGND	
32	DB11	100Ω	**65**	DUMMY		**98**	AGND	
33	DB10	100Ω	**66**	DUMMY		**99**	AGND	

PAD No.	PIN Name	Resistance
101	AGND	
102	AGND	
103	AGND	
104	AGND	
105	DUMMY	
106	DUMMY	Don't care
107	DUMMY	
108	VCOM	
109	VCOM	
110	VCOM	
111	VCOM	5Ω
112	VCOM	
113	VCOM	
114	VCOM	
115	AVCL	
116	AVCL	
117	AVCL	5Ω
118	AVCL	
119	AVCL	
120	AVCL	
121	GVCL	
122	GVCL	50Ω
123	GVCL	
124	GVCL	
125	GVDD	
126	GVDD	50Ω
127	GVDD	
128	DUMMY	
129	DUMMY	Don't care
130	DUMMY	
131	VCL	
132	VCL	50Ω
133	VCL	
134	VCL	

PAD No.	PIN Name	Resistance
135	VCL	
136	AVDD	
137	AVDD	
138	AVDD	5Ω
139	AVDD	
140	AVDD	
141	AVDD	
142	DUMMY	
143	DUMMY	Don't care
144	DUMMY	
145	VDD	
146	VDD	
147	VDD	
148	VDD	
149	VDD	
150	VDD	
151	VDD	
152	VDD	
153	VDD	5Ω
154	VDD	
155	VDD	
156	VDD	
157	VDD	
158	VDD	
159	VDD	
160	VDD	
161	VDD	
162	VDD	
163	DUMMY	
164	DUMMY	
165	DUMMY	Don't care
166	DUMMY	
167	DUMMY	
168	DUMMY	

PAD No.	PIN Name	Resistance
169	DUMMY	
170	DUMMY	
171	DUMMY	
172	DUMMY	
173	DUMMY	
174	DUMMY	
175	DUMMY	
176	DUMMY	Don't care
177	DUMMY	
178	DUMMY	
179	DUMMY	
180	DUMMY	
181	DUMMY	
182	DUMMY	
183	DUMMY	
184	DUMMY	
185	VGL	
186	VGL	
187	VGL	
188	VGL	
189	VGL	50Ω
190	VGL	
191	VGL	
192	VGL	
193	VGL	
194	VGL	
195	AGND	
196	AGND	5Ω
197	AGND	
198	VGH	
199	VGH	
200	VGH	50Ω
201	VGH	
202	VGH	

PAD No.	PIN Name	Resistance
203	VGH	
204	DUMMY	
205	DUMMY	
206	DUMMY	
207	DUMMY	
208	DUMMY	
209	DUMMY	
210	DUMMY	
211	DUMMY	
212	DUMMY	
213	DUMMY	
214	DUMMY	
215	DUMMY	
216	DUMMY	
217	DUMMY	
218	DUMMY	
219	DUMMY	
220	DUMMY	Don't care
221	DUMMY	
222	DUMMY	
223	DUMMY	
224	DUMMY	
225	DUMMY	
226	DUMMY	
227	DUMMY	
228	DUMMY	
229	DUMMY	
230	DUMMY	
231	DUMMY	
232	DUMMY	
233	DUMMY	
234	DUMMY	
235	DUMMY	
236	DUMMY	

PAD No.	PIN Name	Resistance
237	DUMMY	
238	DUMMY	
239	DUMMY	
240	DUMMY	Don't care
241	DUMMY	
242	DUMMY	
243	DUMMY	

Note. Maximum allowable resistance of glass wire and FPC wire must not exceed the value.

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1.. Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VDD	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Digital)	VCC	-0.3 ~ +4.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2.. DC Characteristics

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating Voltage	2.5	2.75	3.3	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Input / Output							
Logic-High Input Voltage	V_{IH}		0.8VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	V_{IL}		VSS		0.2VDDI	V	Note 1
Logic-High Output Voltage	V_{OH}	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	V_{OL}	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Input Leakage Current	I_{LI}	VIN= 0~VDDI	-1		+1	uA	Note 1
Source Driver							
Output Deviation Voltage	V_{DEV}				20	mV	
Output Offset Voltage	V_{OFFSET}				35	mV	Note 2

Table 2 Basic DC Characteristics

Notes:

1. TA= -30 to 85℃.

2. The Max. value is between measured point of source output and gamma setting value.

7.3.. Power Consumption

Ta=25℃, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal Mode	Notes	0.01	2.50	0.01	4.00
Stand-by Mode	Notes	0.01	0.03	0.01	0.05

Table 3 Power Consumption

Notes:

1. All pixels black.

2. The Current Consumption is DC characteristics of ST7781R.

3. Typical: VDDI=1.8V, VDD=2.75V; Maximum: VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V

7.4.. AC Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

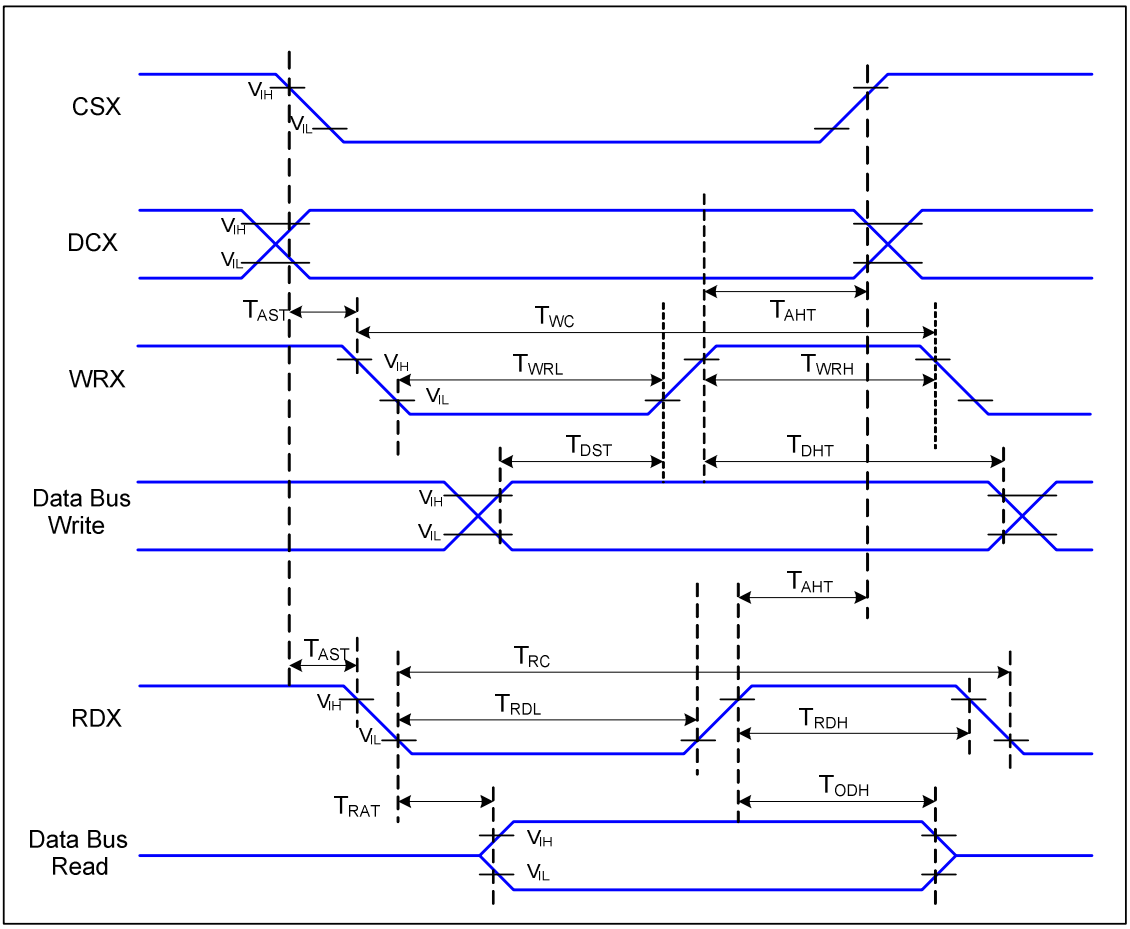


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
DCX	TAST	Address Setup Time	10	-	ns	
	TAHT	Address Hold Time (Write/Read)	5	-	ns	
WRX	TWC	Write Cycle	100	-	ns	
	TWRH	Control Pulse “H” Duration	50	-	ns	
	TWRL	Control Pulse “L” Duration	50	-	ns	
RDX	TRC	Read Cycle (ID)	300	-	ns	When Read ID Data
	TRDH	Control Pulse “H” Duration (ID)	150	-	ns	
	TRDL	Control Pulse “L” Duration (ID)	150	-	ns	
DB[17:0]	TDST	Data Setup Time	10	-	ns	TRAT, TRATFM: 3K

Signal	Symbol	Parameter	Min	Max	Unit	Description
	TDHT	Data Hold Time	15	-	ns	ohm Pull up or Down and 30pF Parallel Cap. To GND. TODH: 3K ohm Pull up or Down.
	TRAT	Read Access Time (ID)	-	100	ns	
	TODH	Output Disable Time	50	-	ns	

Table 4 8080 Parallel Interface Characteristics

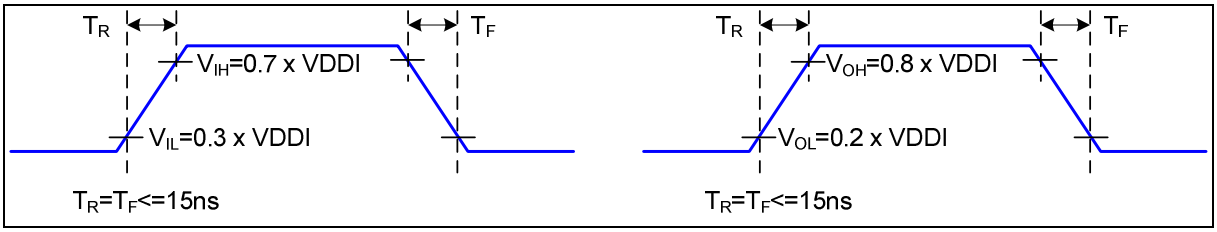


Figure 2 Rising and Falling Timing for I/O Signal

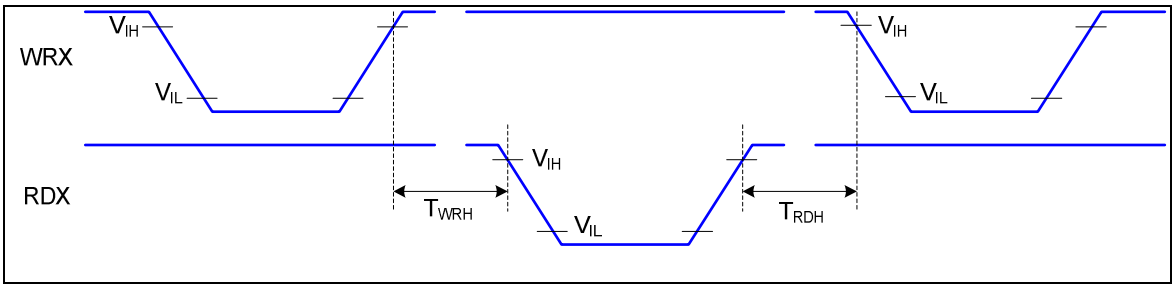


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.2 Serial Data Transfer Interface Characteristics:

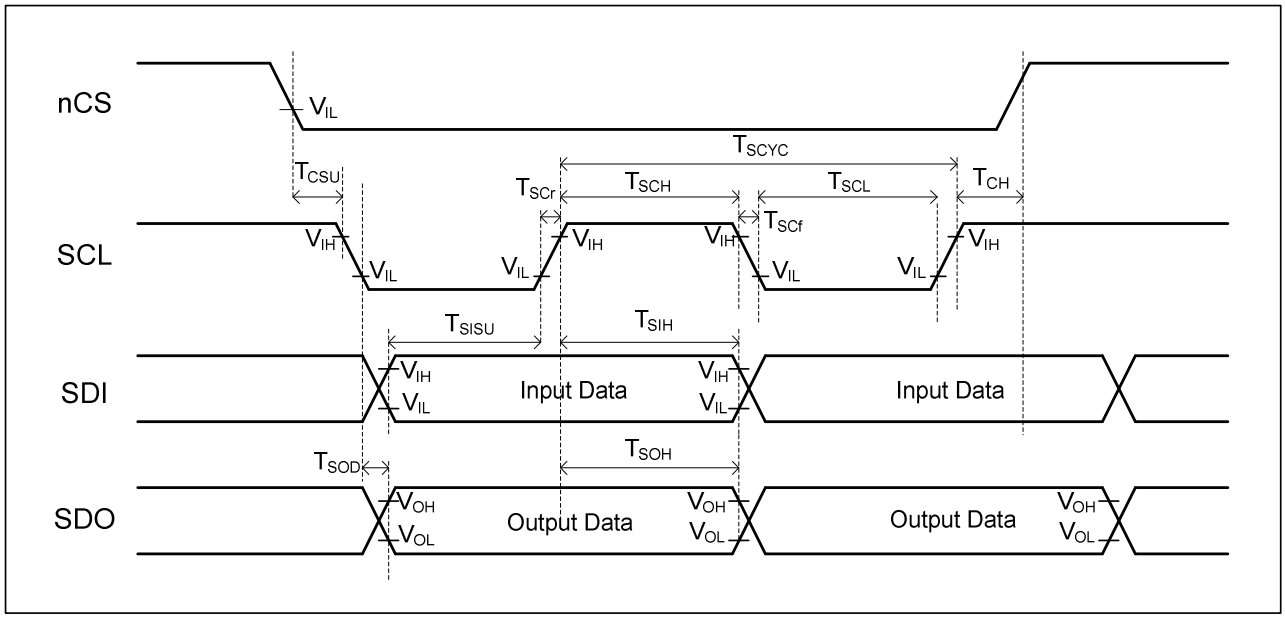


Figure 4 SPI Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	TCSU	Chip Select Setup Time	10		ns	-
	TCH	Chip Select Hold Time	50		ns	
SCL	TSCr ,TSCf	Serial clock rise/fall time		5	ns	
	TSCH	SCL “H” pulse width (Write)	40		ns	
	TSCH	SCL “H” pulse width (Read)	100		ns	
	TSCYC	Serial clock cycle (Write)	100		μs	
	TSCYC	Serial clock cycle (Read)	200		μs	
	TSCL	SCL “L” pulse width (Write)	40		ns	
	TSCL	SCL “L” pulse width (Read)	100		ns	
SDI	TSISU	Serial Input Data Setup Time	20		ns	
	TSIH	Serial Input Data Hold Time	20		ns	
SDO	TSOD	Serial Output Data Setup Time		100	ns	
	TSOH	Serial Output Data Hold Time	5		ns	

Table 5 SPI Interface Characteristics

7.4.3 RGB Interface Characteristics:

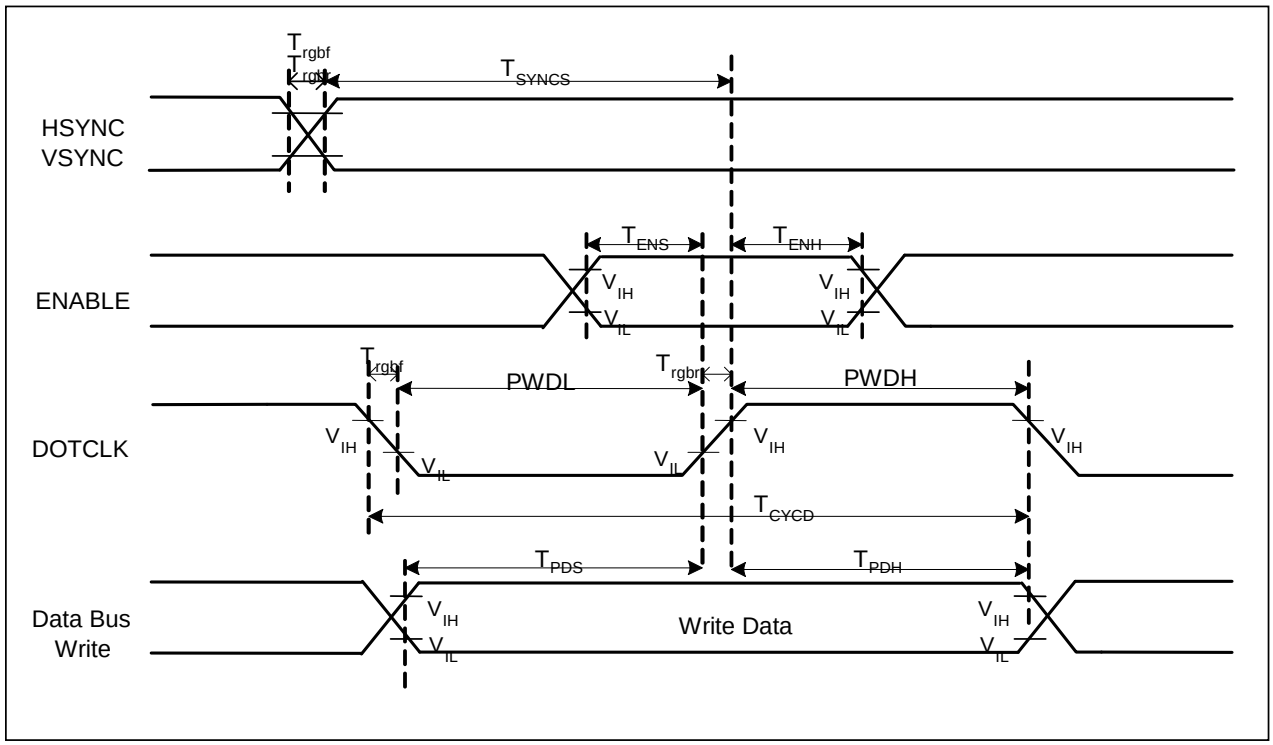


Figure 5 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	TSYNCS	VSYNC, HSYNC Setup Time	0		ns	
	Trghr, Trghf	VSYNC, HSYNC Rise/Fall time		25	ns	
ENABLE	TENS	Enable Setup Time	10		ns	
	TENH	Enable Hold Time	10		ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	40		ns	
	PWDL	DOTCLK Low-level Pulse Width	40		ns	
	TCYCD	DOTCLK Cycle Time	100		ns	
	Trghr, Trghf	DOTCLK Rise/Fall time		25	ns	
DB	TPDS	PD Data Setup Time	10		ns	
	TPDH	PD Data Hold Time	40		ns	

Table 6 18/16 Bits RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	TSYNCS	VSYNC, HSYNC Setup Time	0		ns	
	Trghr, Trghf	VSYNC, HSYNC Rise/Fall time		25	ns	
ENABLE	TENS	Enable Setup Time	10		ns	
	TENH	Enable Hold Time	10		ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30		ns	
	PWDL	DOTCLK Low-level Pulse Width	30		ns	
	TCYCD	DOTCLK Cycle Time	80		ns	
	Trghr, Trghf	DOTCLK Rise/Fall time		25	ns	
DB	TPDS	PD Data Setup Time	10		ns	
	TPDH	PD Data Hold Time	30		ns	

Table 7 6 Bits RGB Interface Timing Characteristics

8 INTERFACE

8.1.. MPU Interface Type Selection

ST7781R supports 8/16/9/18 bit parallel data bus for 8080 series CPU, RGB serial interfaces. Selection of these interfaces are set by IM[3:0] pins as shown below.

IM3	IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	0	1	0	8080 MCU 16-bit Parallel	16-bit Read Data and 8-bit Read Parameter
0	0	1	1	8080 MCU 8-bit Parallel	8-bit Read Data and 8-bit Read Parameter
0	1	0	ID	Serial Peripheral Interface(SPI)	16-bit Command and 16 / 24bit Parameter
0	1	1	--	Setting invalid	
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	0	1	0	8080 MCU 18-bit Parallel	18-bit Read Data and 8-bit Read Parameter
1	0	1	1	8080 MCU 9-bit Parallel	9-bit Read Data and 8-bit Read Parameter
1	1	--	--	Setting invalid	

Table 8 Interface Type Selection

8.2.. 8080-Series MCU Write Cycle Sequence

The write cycle means that the host writes information (command / data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[17:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

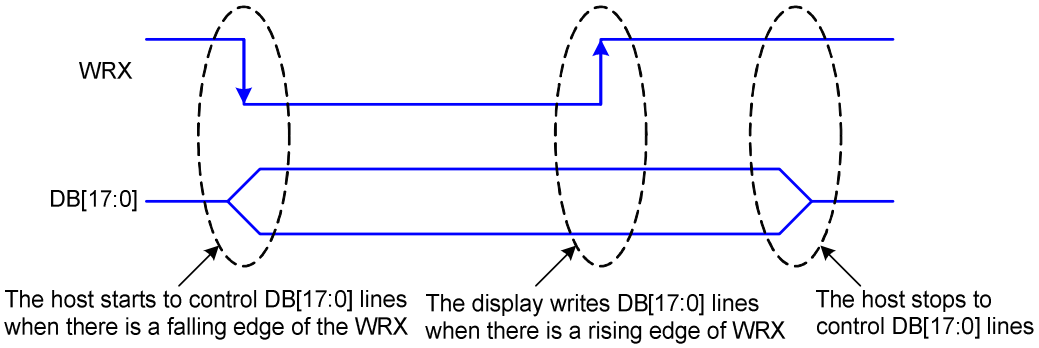


Figure 6 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

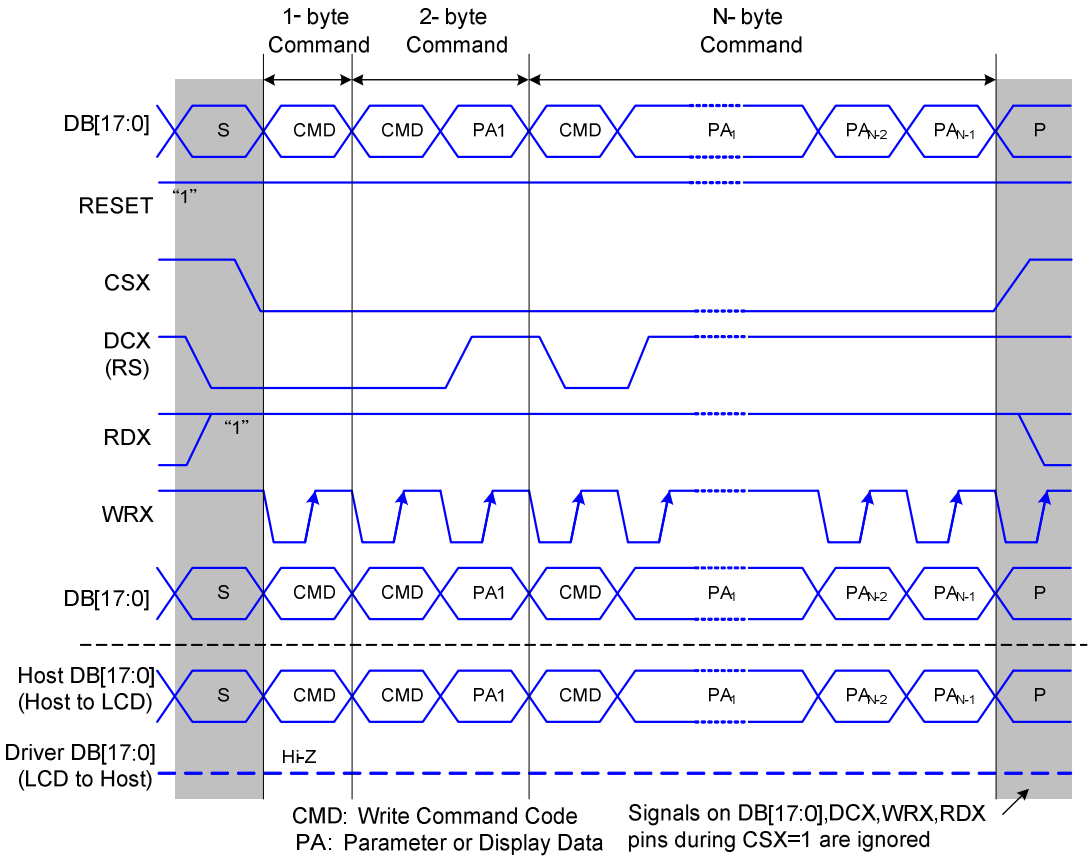


Figure 7 8080-Series Parallel Bus Protocol, Write to Register or Display RAM

8.2.1 8080-18 bits Interface Write Data Format

The 8080-18bits interface is selected by setting the IM [3:0] =”1010”.This mode only 262k colors format in display. In this interface write instructions and DRAM method following figure.

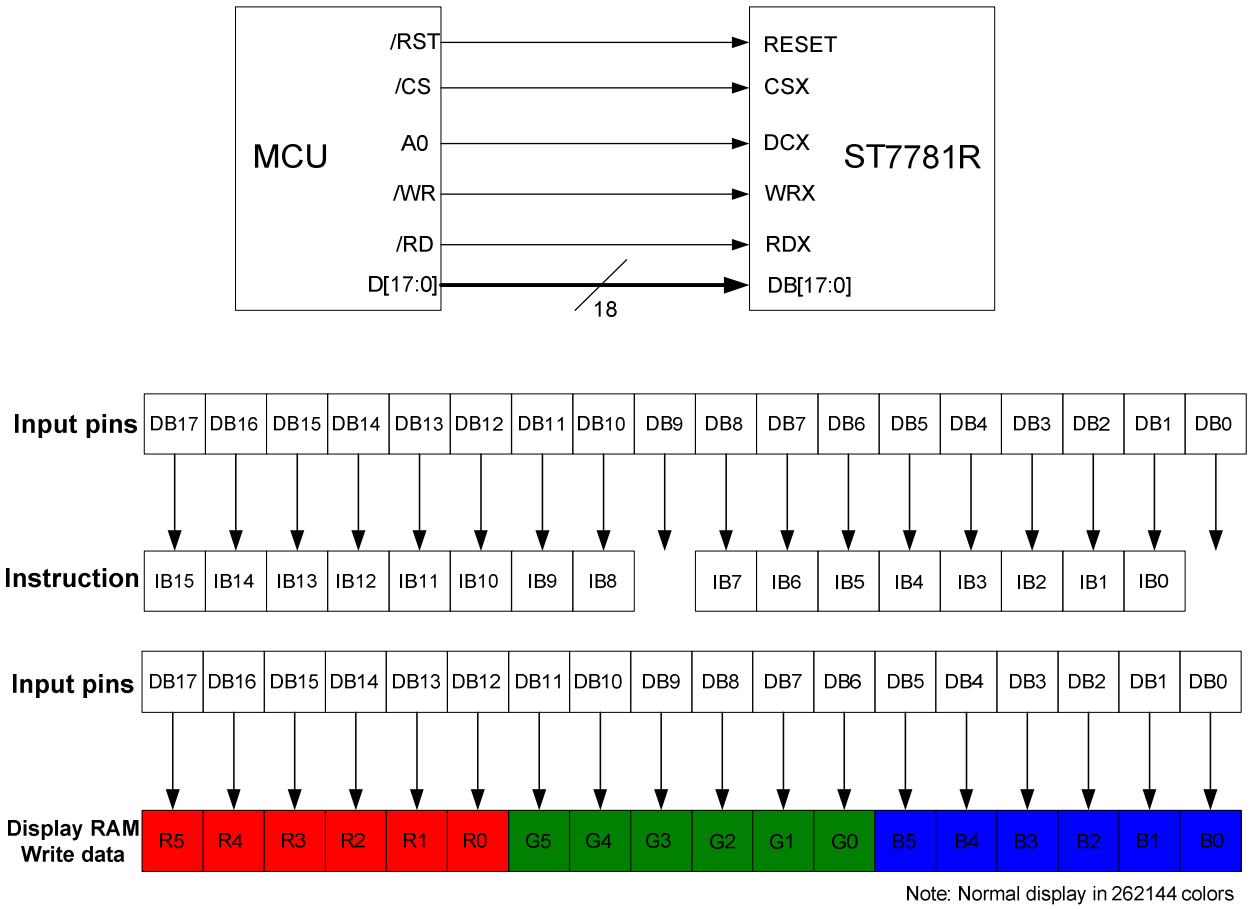


Figure 8 8080-18 bits Interface Data Format (Command Write/DRAM Write)

8.2.2 8080-16 bits Interface Write Data Format

The 8080-16bits interface is selected by setting IM [3:0] =”0010”.The mode can display 262k or 65k colors format. When the 262k color format is display, two transfers mode is used (first transfer: 2 bits, second transfer: 16 bits or first transfer: 16 bits, second transfer: 2 bits).

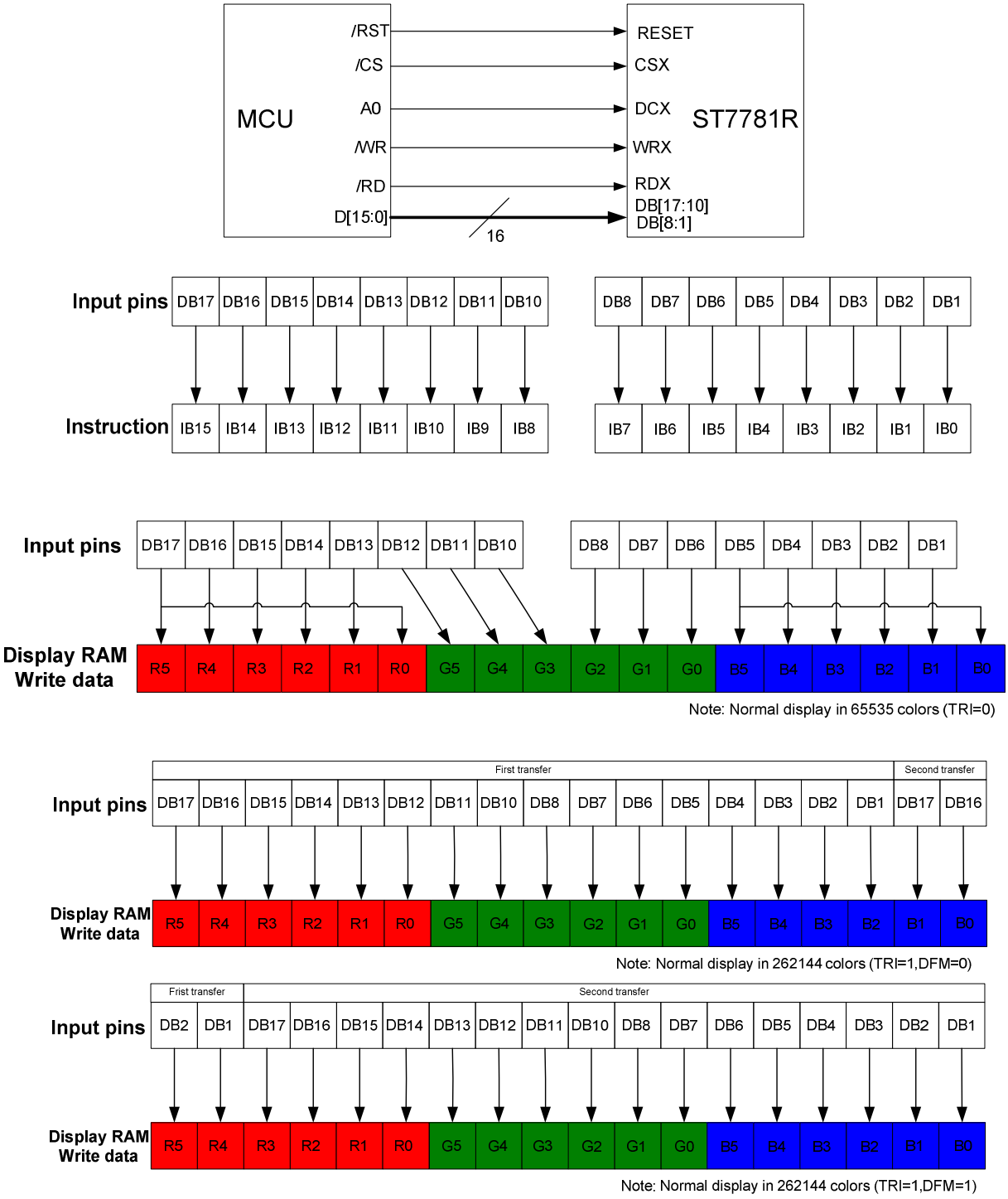


Figure 9 8080-16 bits Interface Data Format (Command Write/Display RAM Write)

8.2.3 8080-9 bits Interface Write Data Format

The 8080-9bits interface is selected by setting the IM [3:0] = “1011” and the DB [17:9] pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte and lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB [8:0] pins must be tied to either VDDI or DGND.

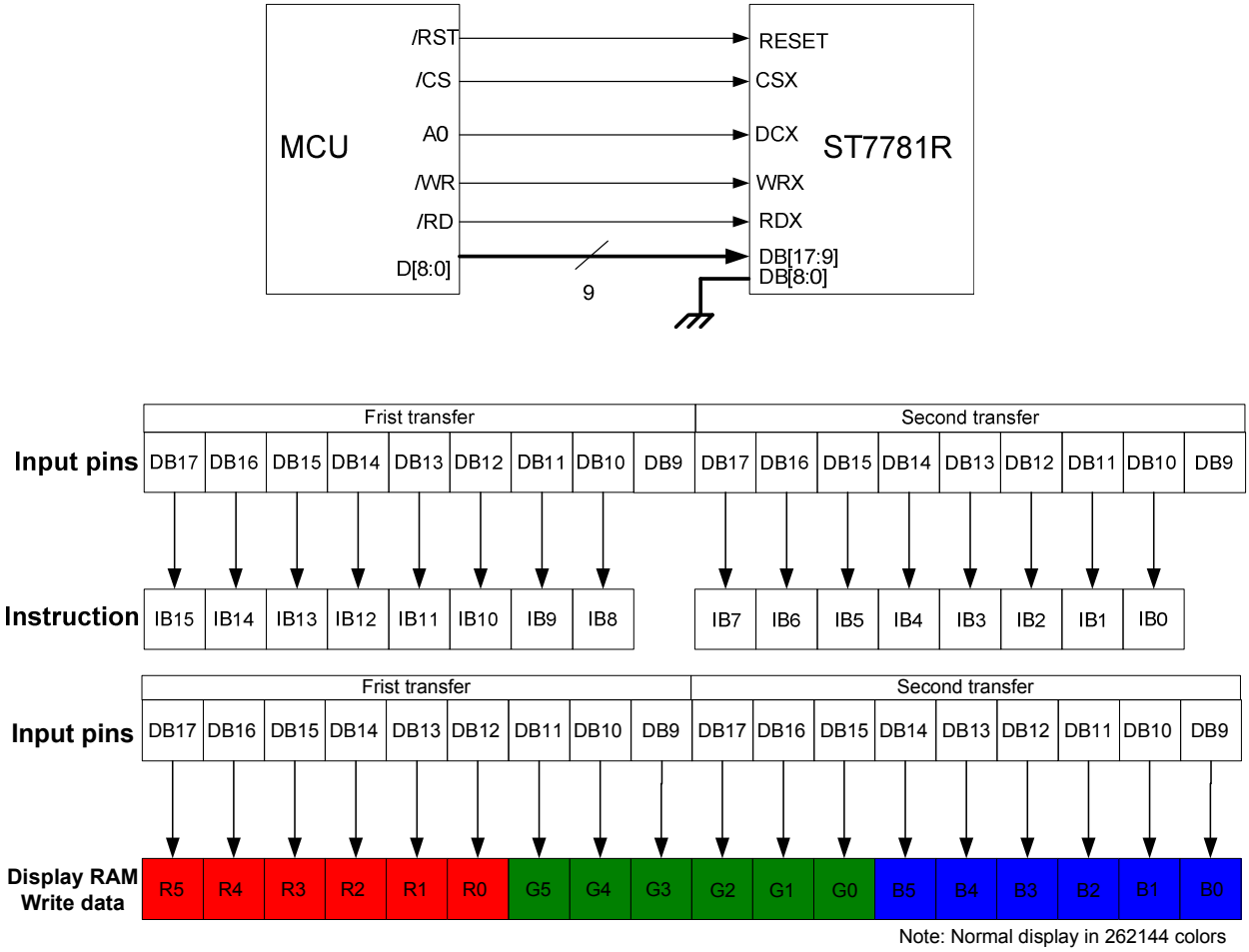
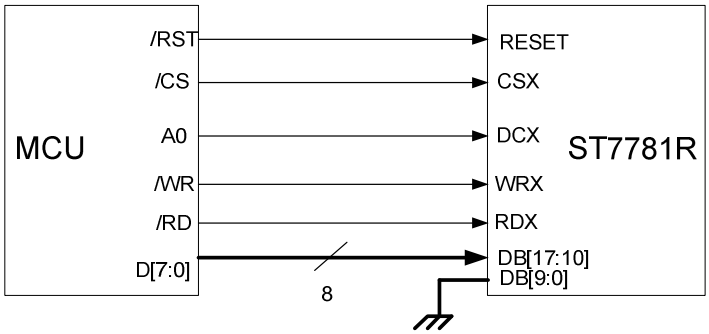
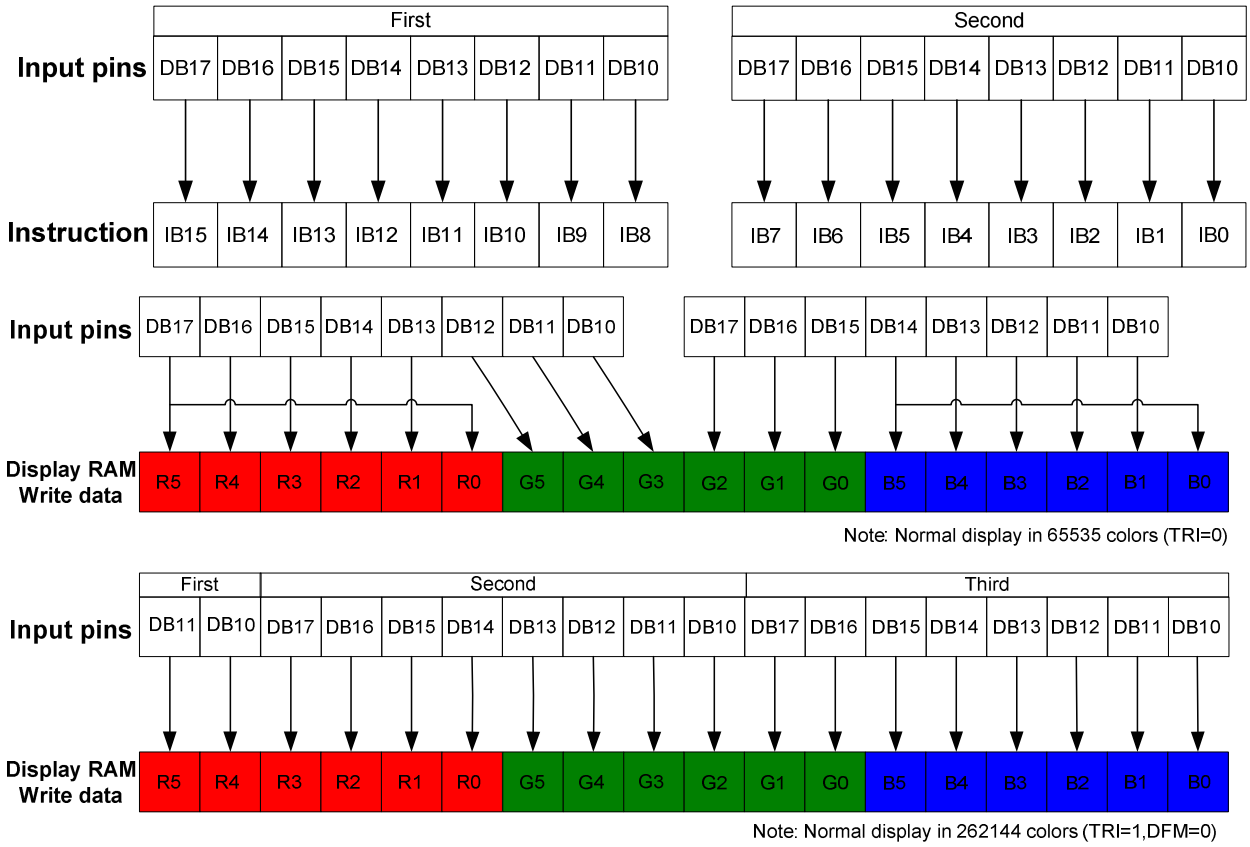


Figure 10 8080-9 bits Interface Data Format (Command Write/Display RAM Write)

8.2.4 8080-8 bits Interface Write Data Format

The 8080 8-bit interface is selected by setting the IM [3:0] as “0011” and the DB [17:10] pins are used to transfer the data. The mode can display 262k or 65k colors format. When writing the 16-bit register, the data is divided into upper byte lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into DRAM. The unused DB [9:0] pins must be tied to either VDDI or DGND.





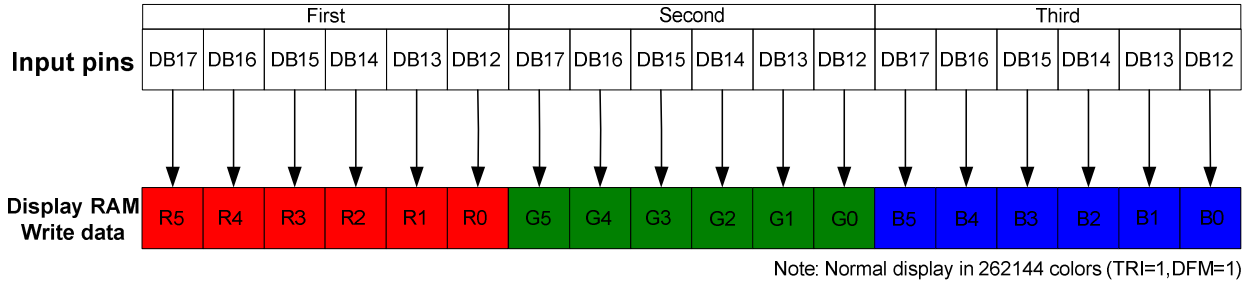


Figure 11 8080-8 bits interface data format (command write/Display RAM write)

8.2.5 8080-series MCU Read Cycle Sequence

The read cycle (RDX “1”- “0”- “1” sequence) means that the host reads information from display via interface. The driver sends data (DB [17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

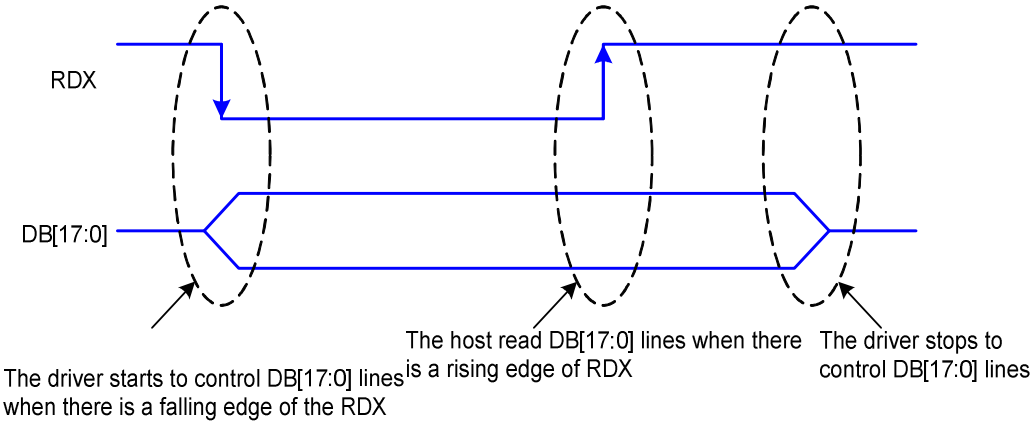


Figure 12 8080-Series RDX Protocol

Note1: RDX is an unsynchronized signal (It can be stopped)

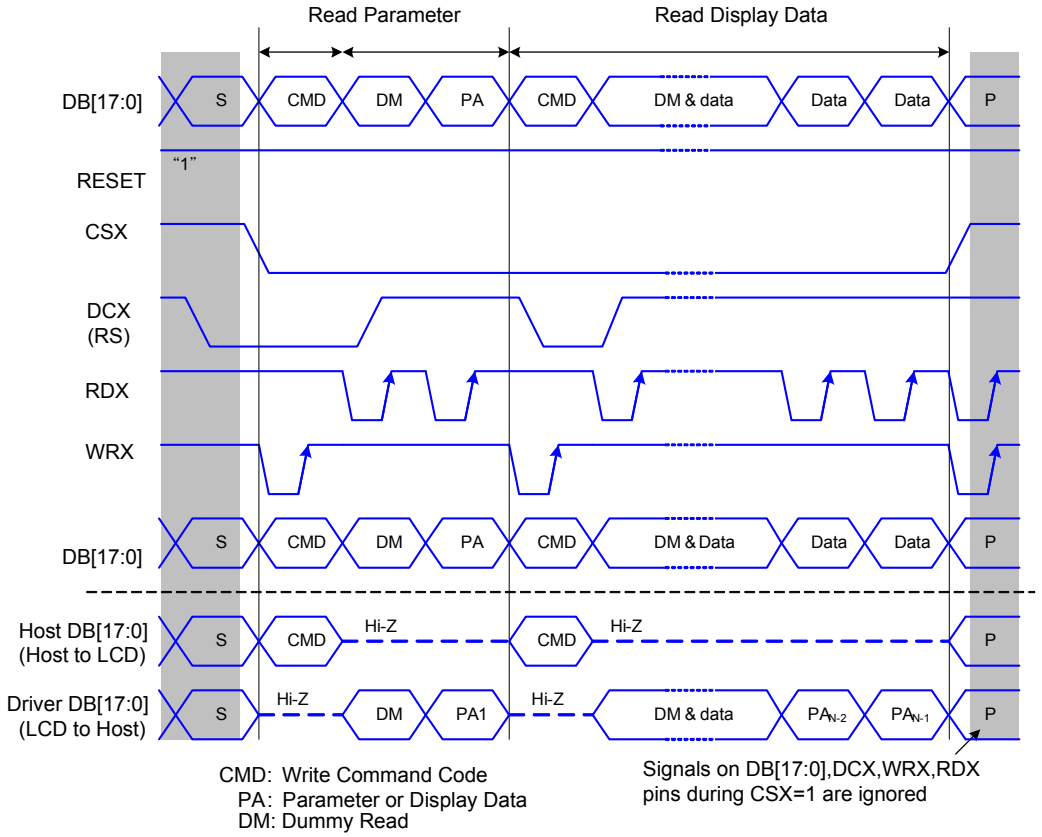
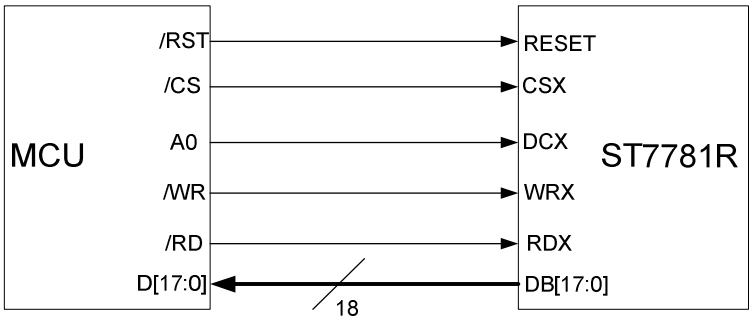


Figure 13 8080-series parallel bus protocol, read data from register or display RAM

8.2.6 8080-18bits interface read data format



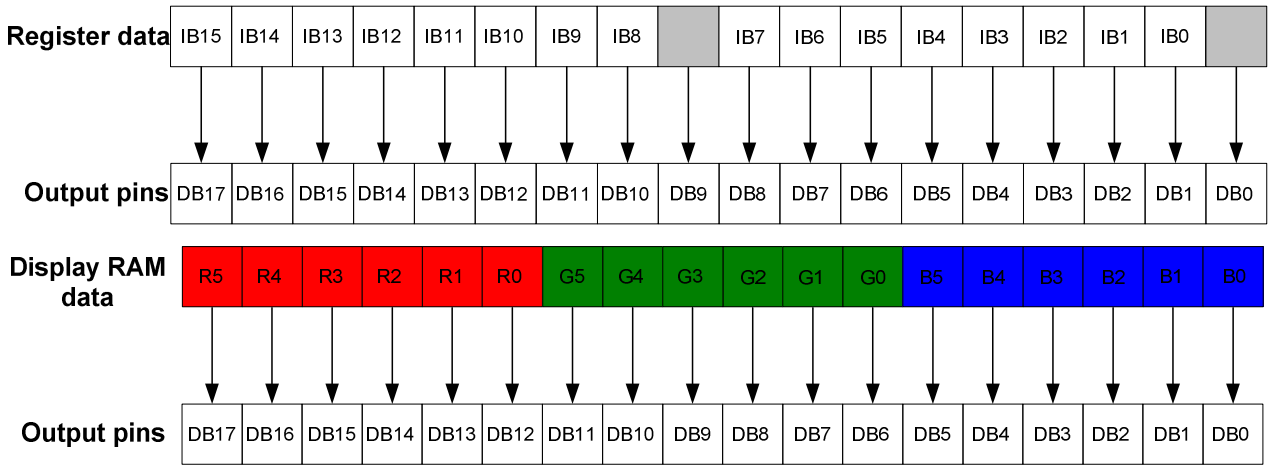


Figure 14 8080-18 bits Interface Data Format (Command Read/Display RAM Read)

8.2.7 8080-16bits Interface Read Data Format

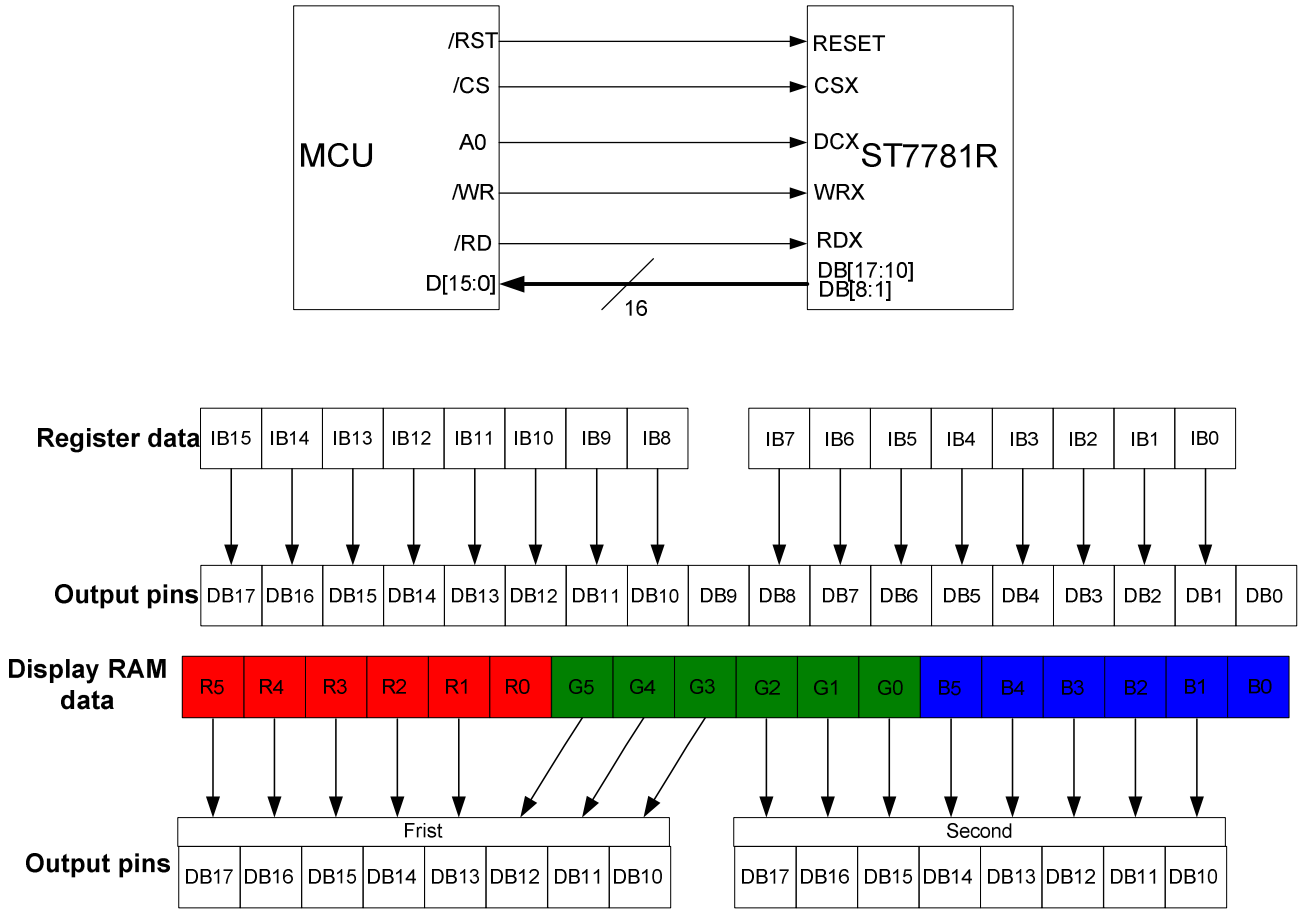


Figure 15 8080-16 bits Interface Data Format (Command Read/Display RAM Read)

8.2.8 8080-9bits Interface Read Data Format

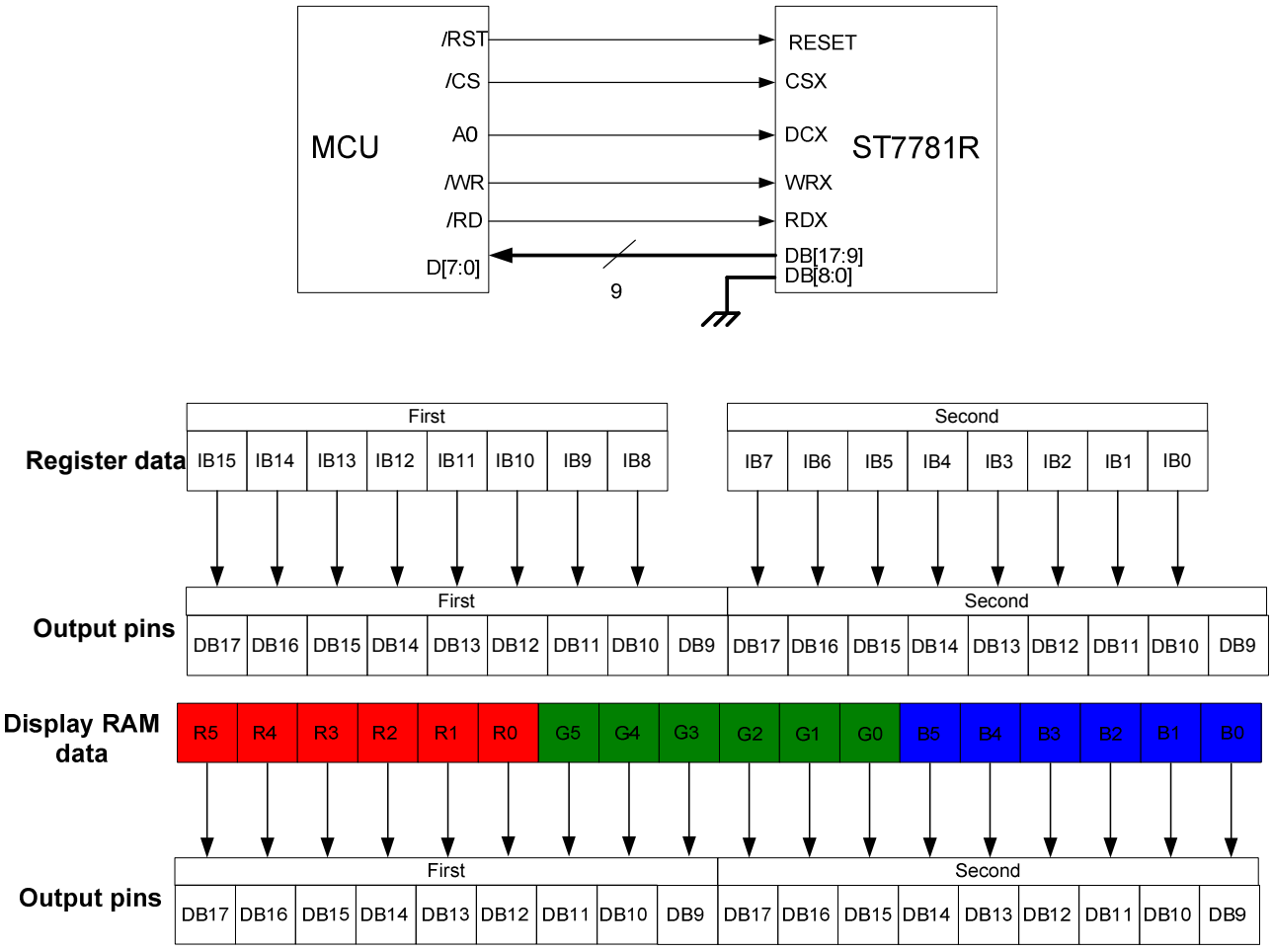


Figure 16 8080-9 bits Interface Data Format (Command Read/Display RAM Read)

8.2.9 8080-8bits Interface Read Data Format

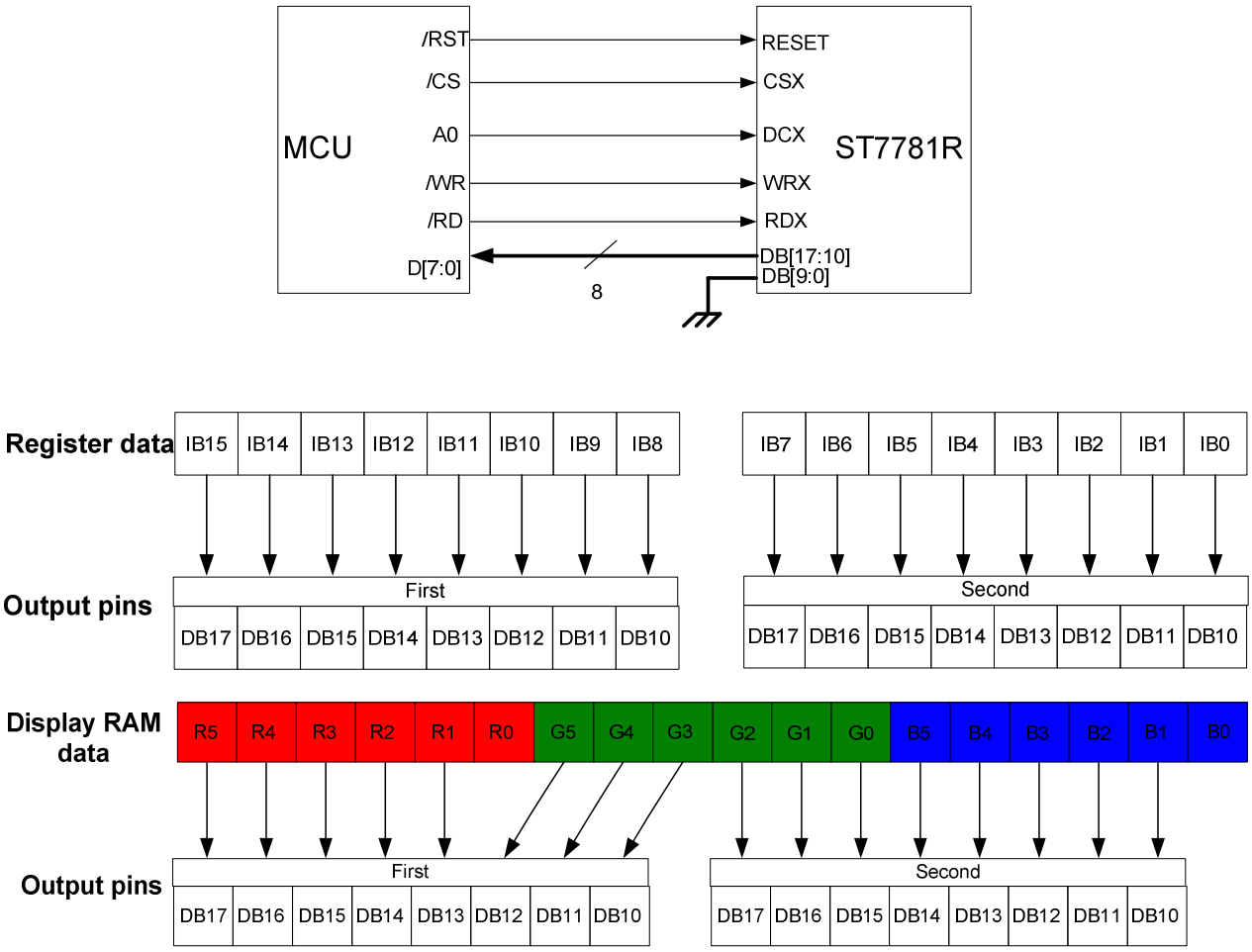


Figure 17 8080-8 bits Interface Data Format (Command Read/Display RAM Read)

GS = '1'	GS = '0'	SS = '0'	S1	S2	S3	S4	S5	S6	------	S715	S716	S717	S718	S719	S720
		SS = '1'	S718	S719	S720	S715	S716	S717	-------	S4	S5	S6	S1	S2	S3
		BGR='0'	R	G	B	R	G	B	-------	R	G	B	R	G	B
		BGR='1'	B	G	R	B	G	R		B	G	R	B	G	R
G320	G1	X Address	"0000"h			"0001"h			-------	"00EE"h			"00EF"h		
		Y Address	"0000"h			"0000"h				"0000"h			"0000"h		
G319	G2	X Address	"0000"h			"0001"h			-------	"00EE"h			"00EF"h		
		Y Address	"0001"h			"0001"h				"0001"h			"0001"h		
|	|	|	|			|			-------	|			|		
|	|	|	|			|				|			|		
|	|	|	|			|				|			|		
|	|	|	|			|				|			|		
G2	G319	X Address	"0000"h			"0001"h			-------	"00EE"h			"00EF"h		
		Y Address	"013E"h			"013E"h				"013E"h			"013E"h		
G1	G320	X Address	"0000"h			"0001"h			-------	"00EE"h			"00EF"h		
		Y Address	"013F"h			"013F"h				"013F"h			"013F"h		

Figure 18 DRAM Address Map Table

Note:

X Address Start Instruction：R50h

X Address End Instruction：R51h

Y Address Start Instruction：R52h

Y Address End Instruction：R53h

SS/GS Setting Instruction：R01h

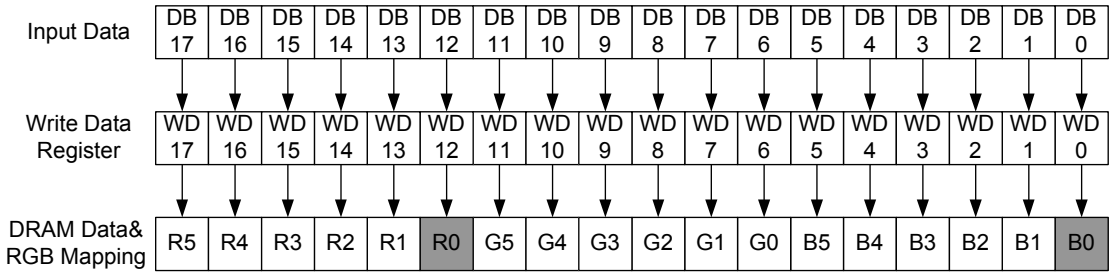
BGR Setting Instruction：R03h

8.3.. RGB Input Interface

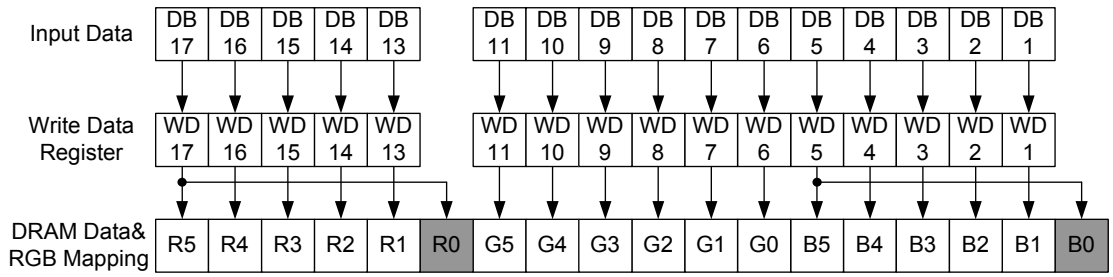
The RGB Interface mode for ST7781R is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface Mode	Data pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

18-bit RGB Interface (262K colors)



16-bit RGB Interface (65K colors)



6-bit RGB Interface (262K colors)

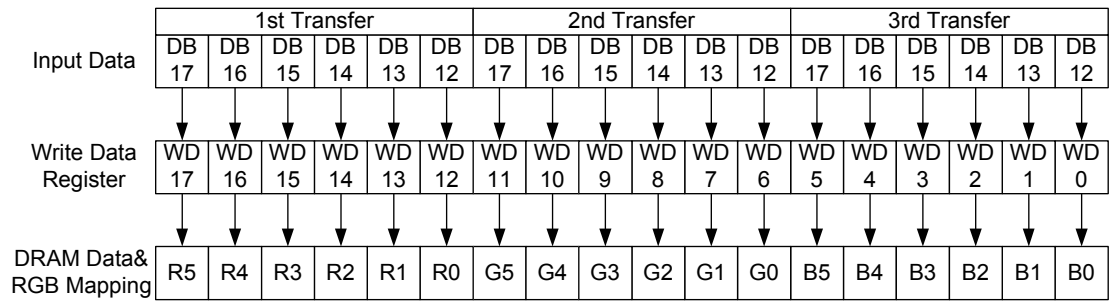


Figure 19 RGB Interface Data Format

8.3.1 RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function and high-speed write mode (HWM = 1). The back porch and front porch are used to set the RGB interface timing.

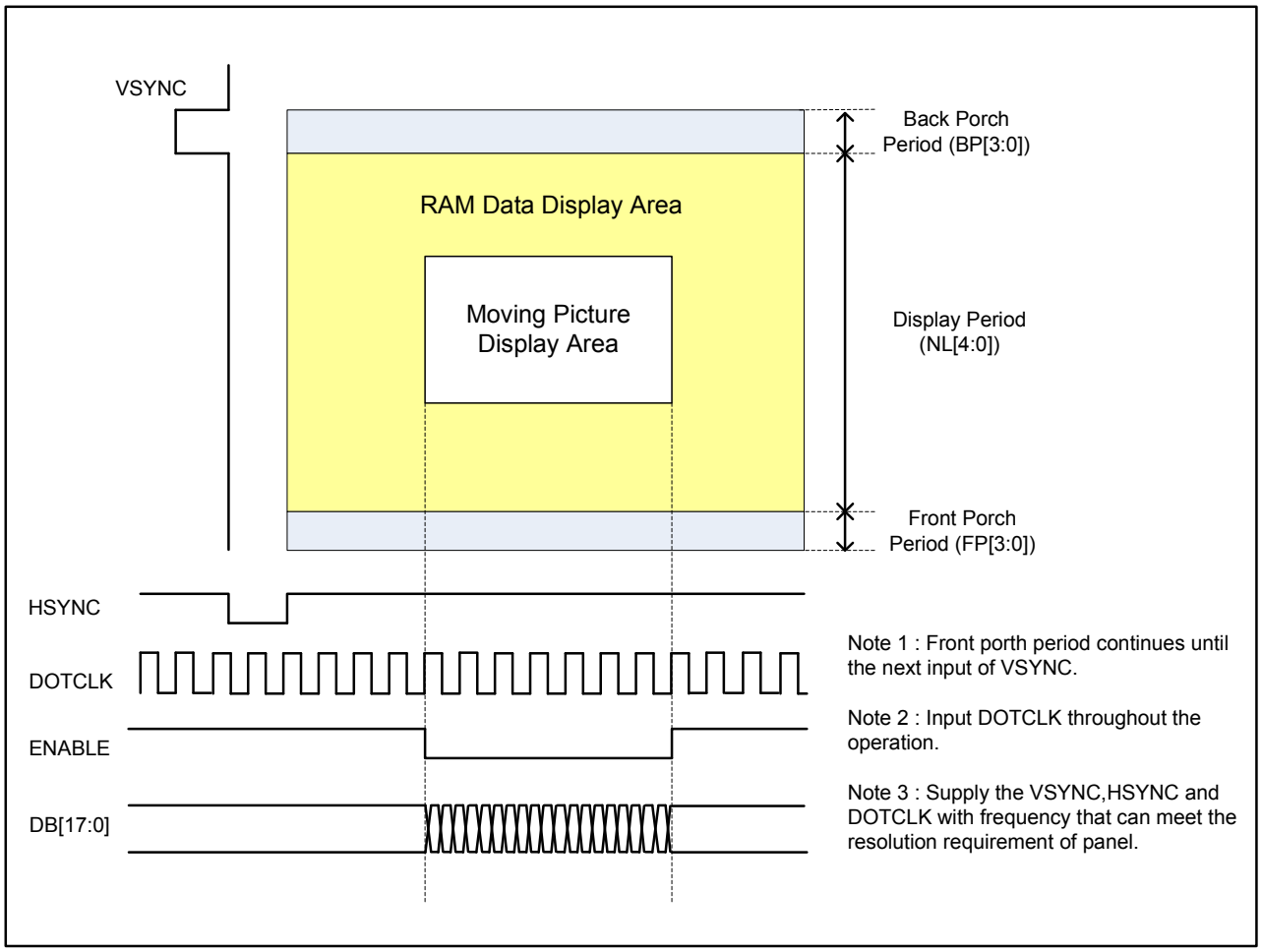


Figure 20 DRAM Access Area by RGB Interface

8.3.2 RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.

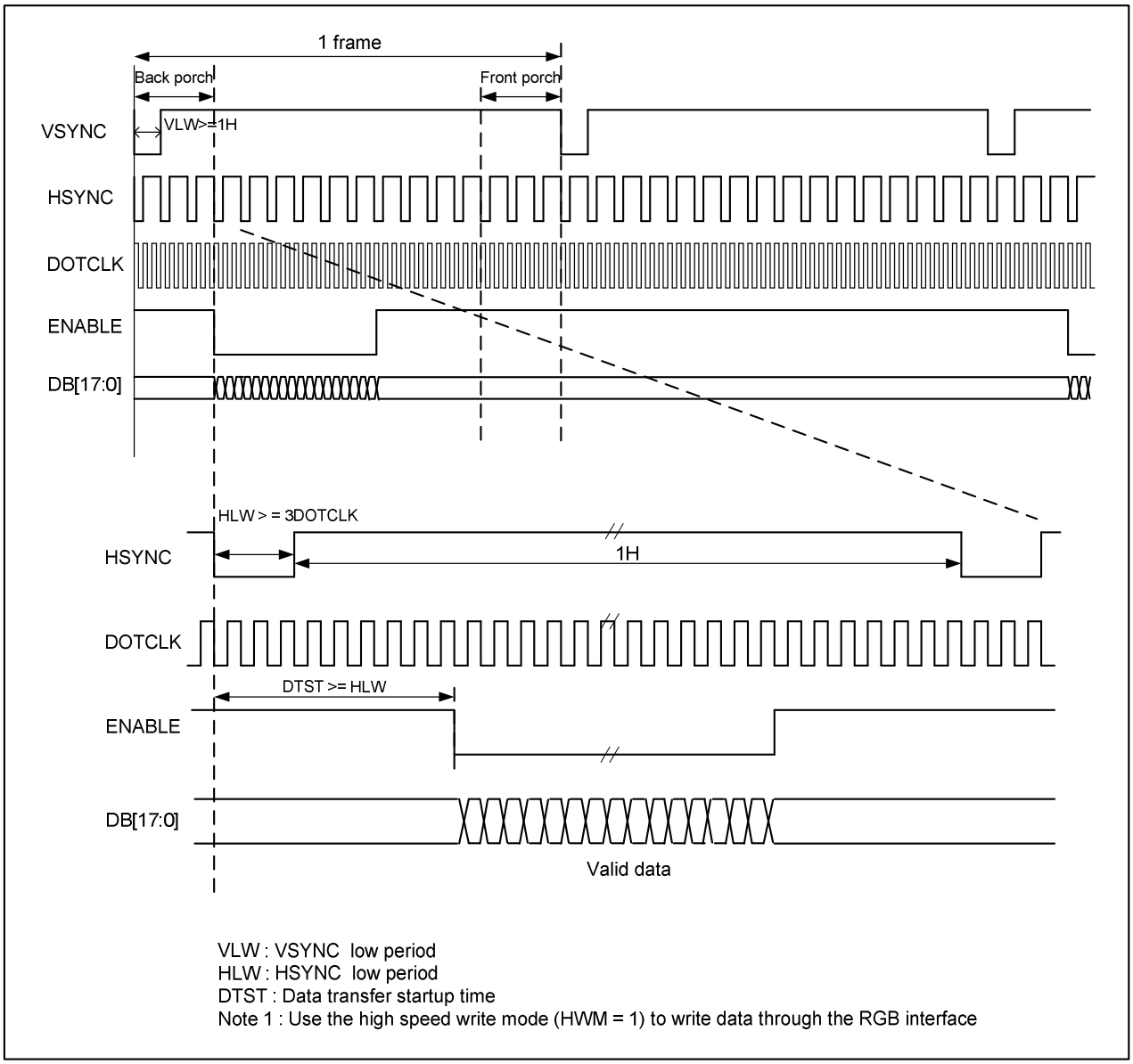
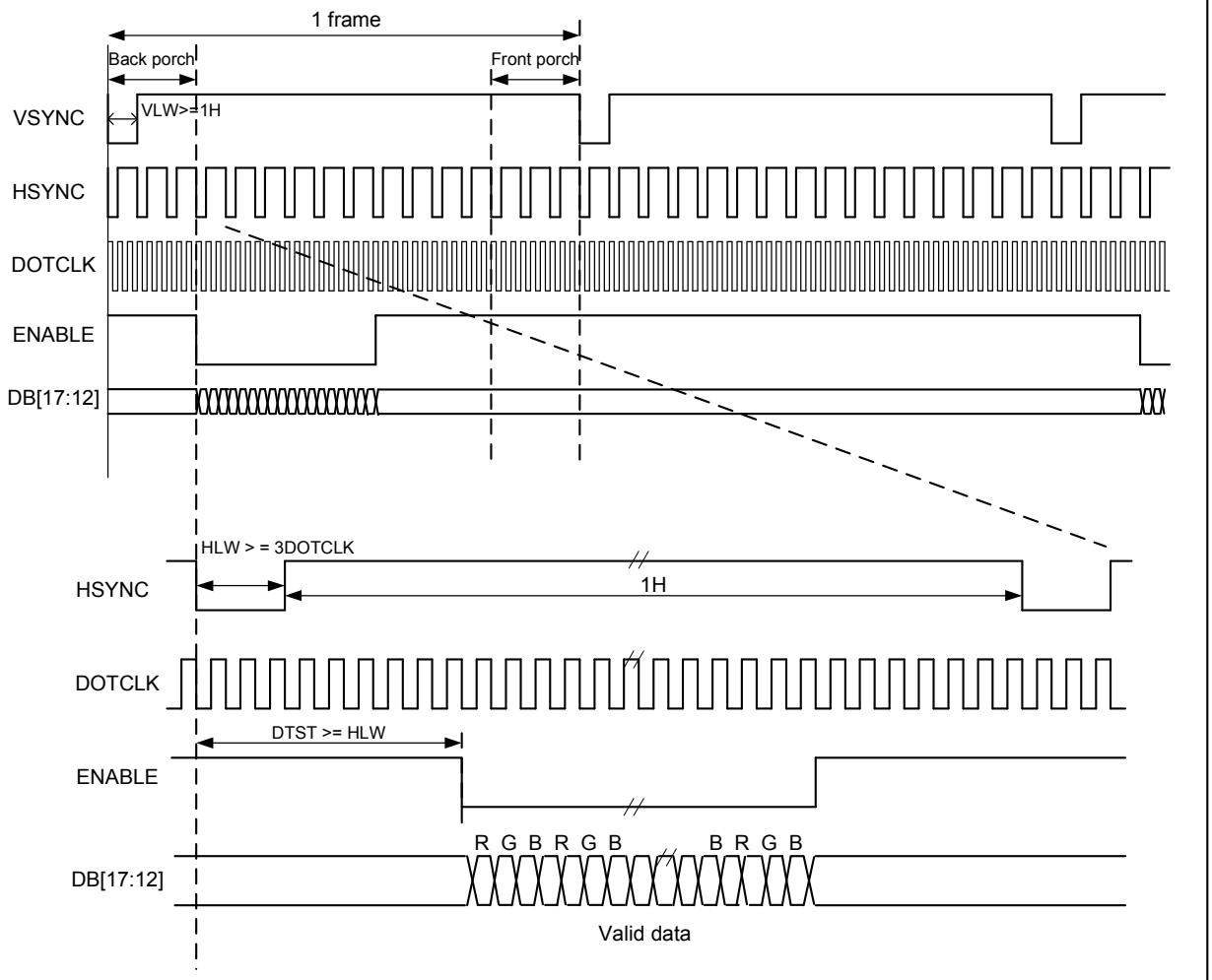


Figure 21 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as follows.



VLW : VSYNC low period
HLW : HSYNC low period
DTST : Data transfer startup time
Note 1 : Use the high speed write mode (HWM = 1) to write data through the RGB interface.
Note 2 : In 6-bite RGB interface mode , each dot of one pixel (R , G and B) is transferred in synchronization with DOTCLKs.
Note 3 : In 6-bite RGB interface mode , set the cycles of VSYNC , HSYNC and ENABLE to 3 multiples of DOTCLKs.

Figure 22 Timing chart of signals in 6-bit RGB interface mode

8.3.3 Moving Picture Mode

ST7781R has the RGB interface to display moving picture and incorporates DRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of DRAM.
- The DRAM is updated only the moving picture area.
- It can contribute to lower the power consumption of the system by reducing data transfer.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

ST7781R allows DRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal DRAM in synchronization with DOTCLK while ENABLE signal is “Low”. When write data to the internal DRAM by the system interface, set ENABLE(“High”) to stop write data via RGB interface. Then set RM = “0” to enable RAM access via system interface. When restart RAM access in RGB interface mode, wait one read/write cycle, set RM = “1” and then the index register (R22h) to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal DRAM.

The following figure illustrates the operation of the ST7781R when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

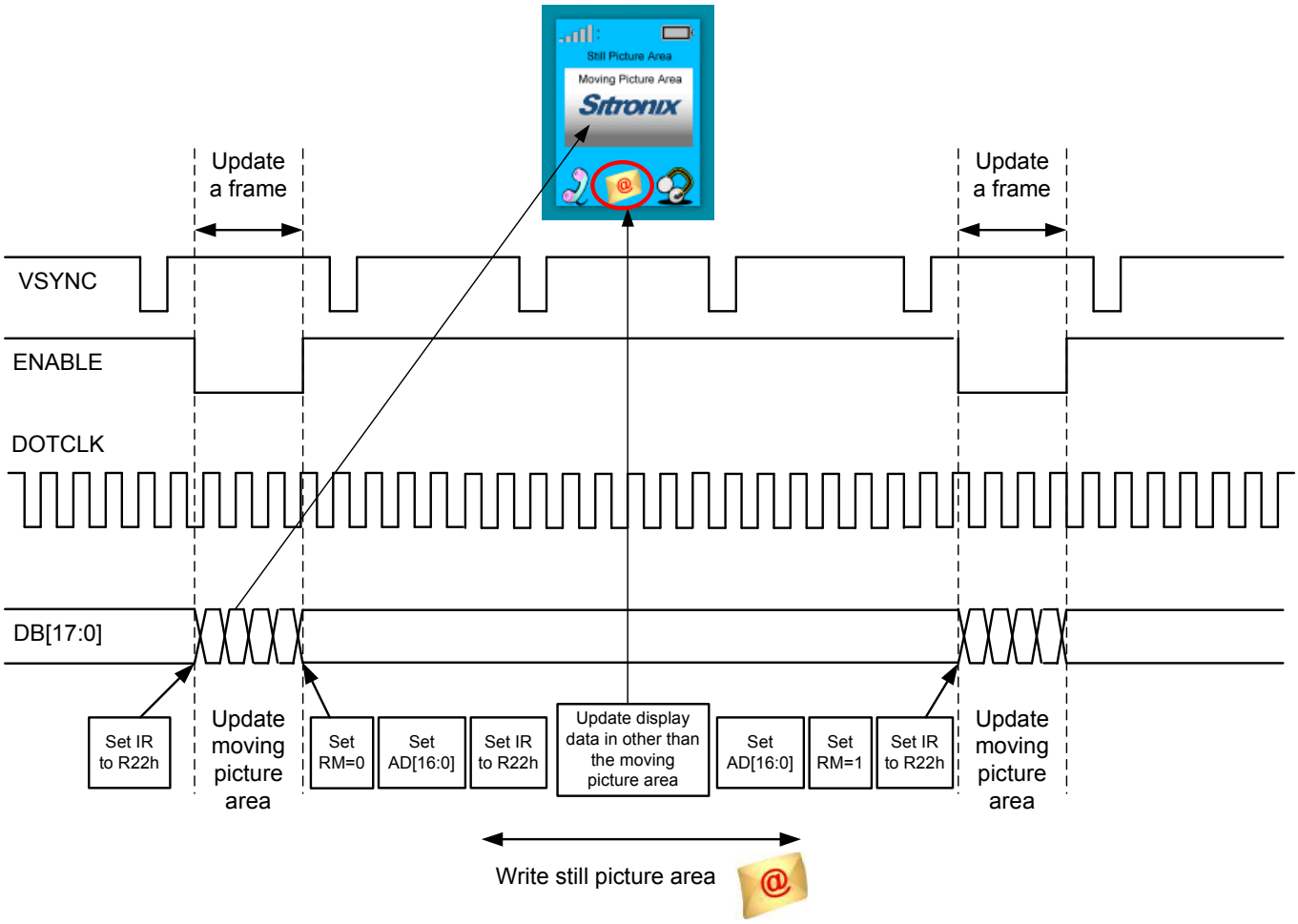
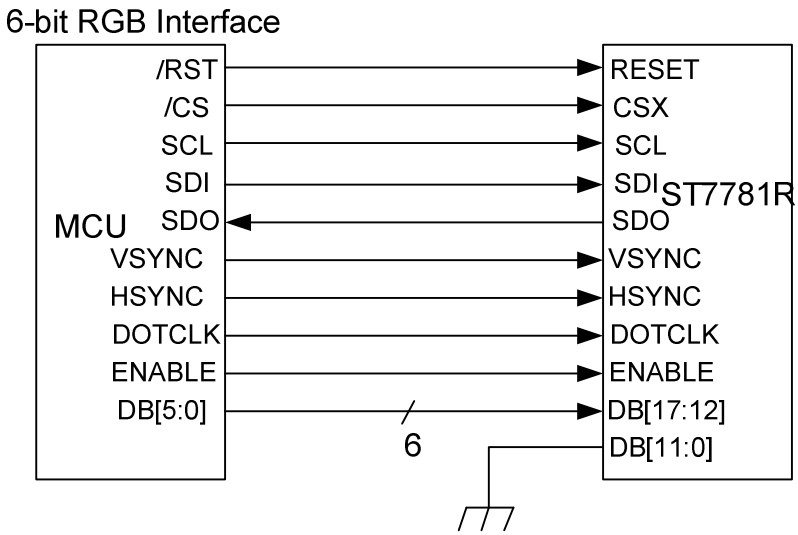


Figure 23 Example of update the still and moving picture

8.3.4 6-bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal DRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at GND level. Registers can be set by the system interface (i80/SPI).



RGB Interface With 6-bit Data Bus (RIM=10)

	1st Transfer						2nd Transfer						3rd Transfer					
Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Figure 24 Example of 6-bit RGB interface data format

Data transfer synchronization in 6-bit RGB interface mode

St7781R has counters to count the first, second, third 6 bit transfers via 6-bit RGB interface. The transfer counters are always reset to first data on the falling edge of VSYNC from the next frame period. If a mismatch data transfer occurs, the correct data transfer will be restart via 6 bit interface in next frame period. When data transfer is consecutively in moving picture operation, this function can help the display system restoring normal display operation and minimizes effects in occurring mismatch data transfer.

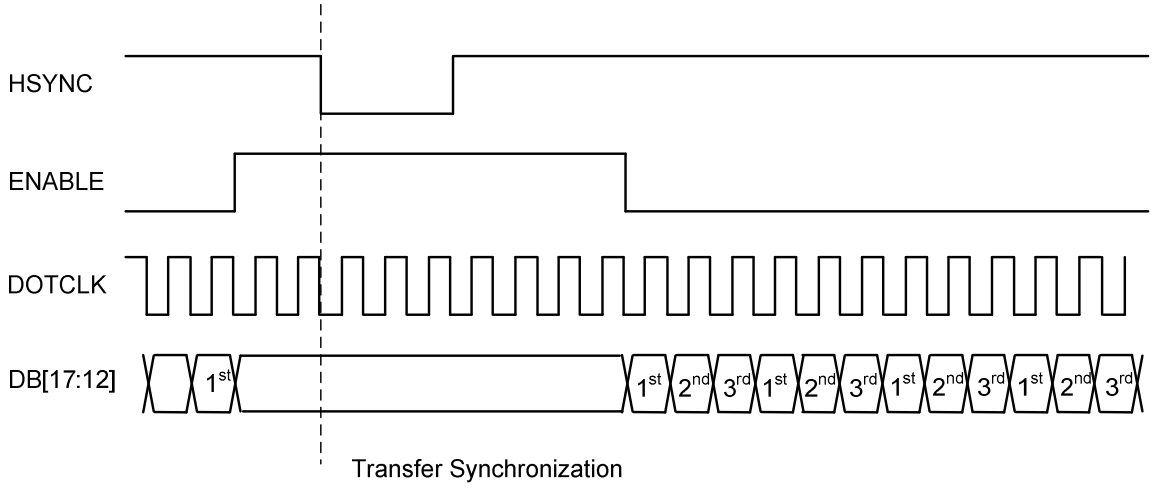
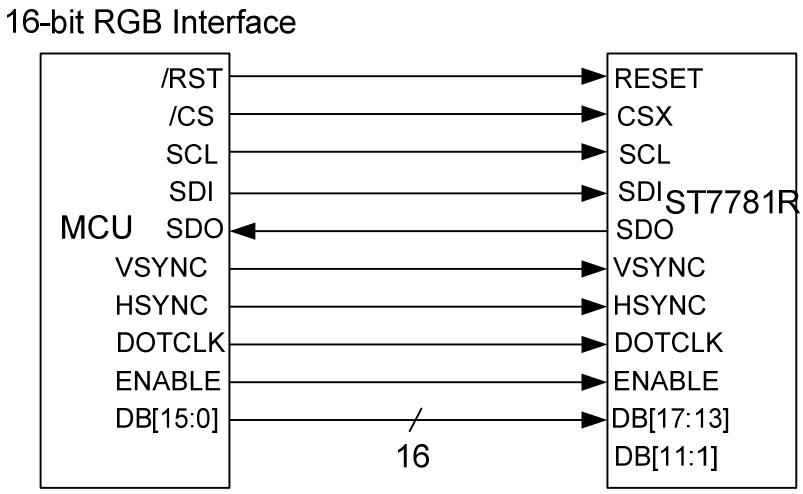


Figure 25 6-bit Transfer Synchronization

8.3.5 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB[17:13], DB[11:1]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



16-bit RGB Interface (65K colors)

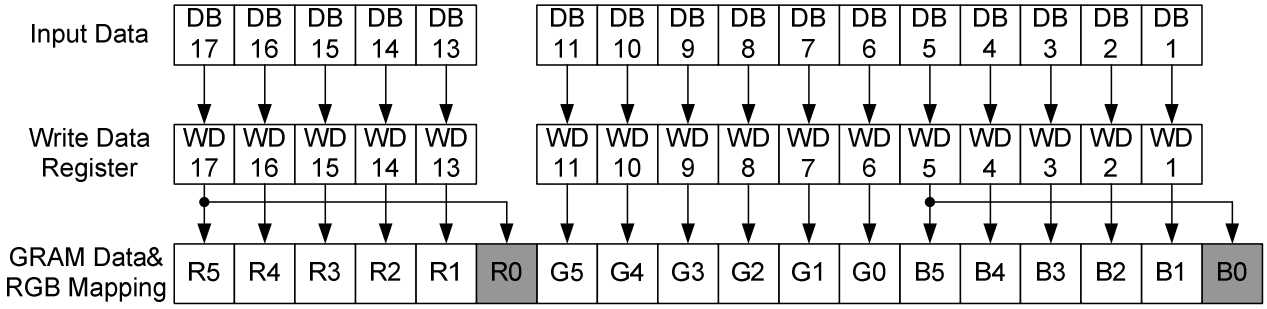
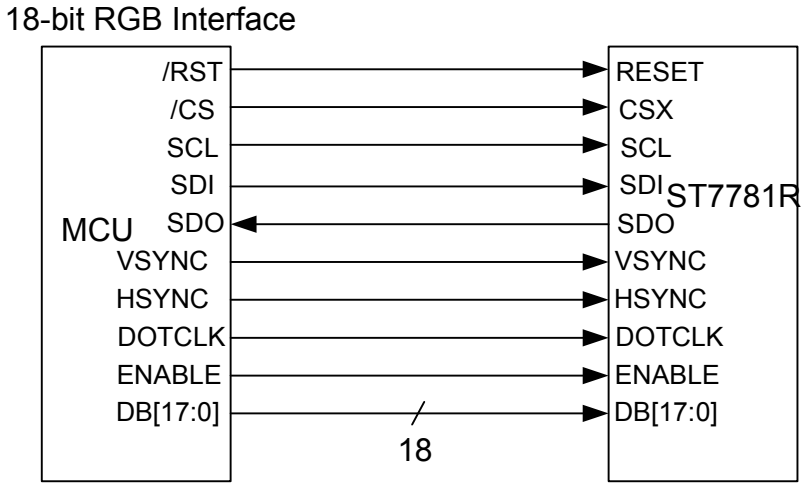


Figure 26 Example of 16-Bit RGB Interface and Data Format

8.3.6 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



RGB Interface With 18-bit Data Bus

	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 4	DB 2	DB 1	DB 0
Input Data																		
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Figure 27 Example of 18-bit RGB Interface and Data Format

Notes to external display in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

3. In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

4. In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

5. In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

6. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

8. In RGB interface mode, a RAM address (AD[16:0]) is set in the address counter every frame on the falling edge of VSYNC.

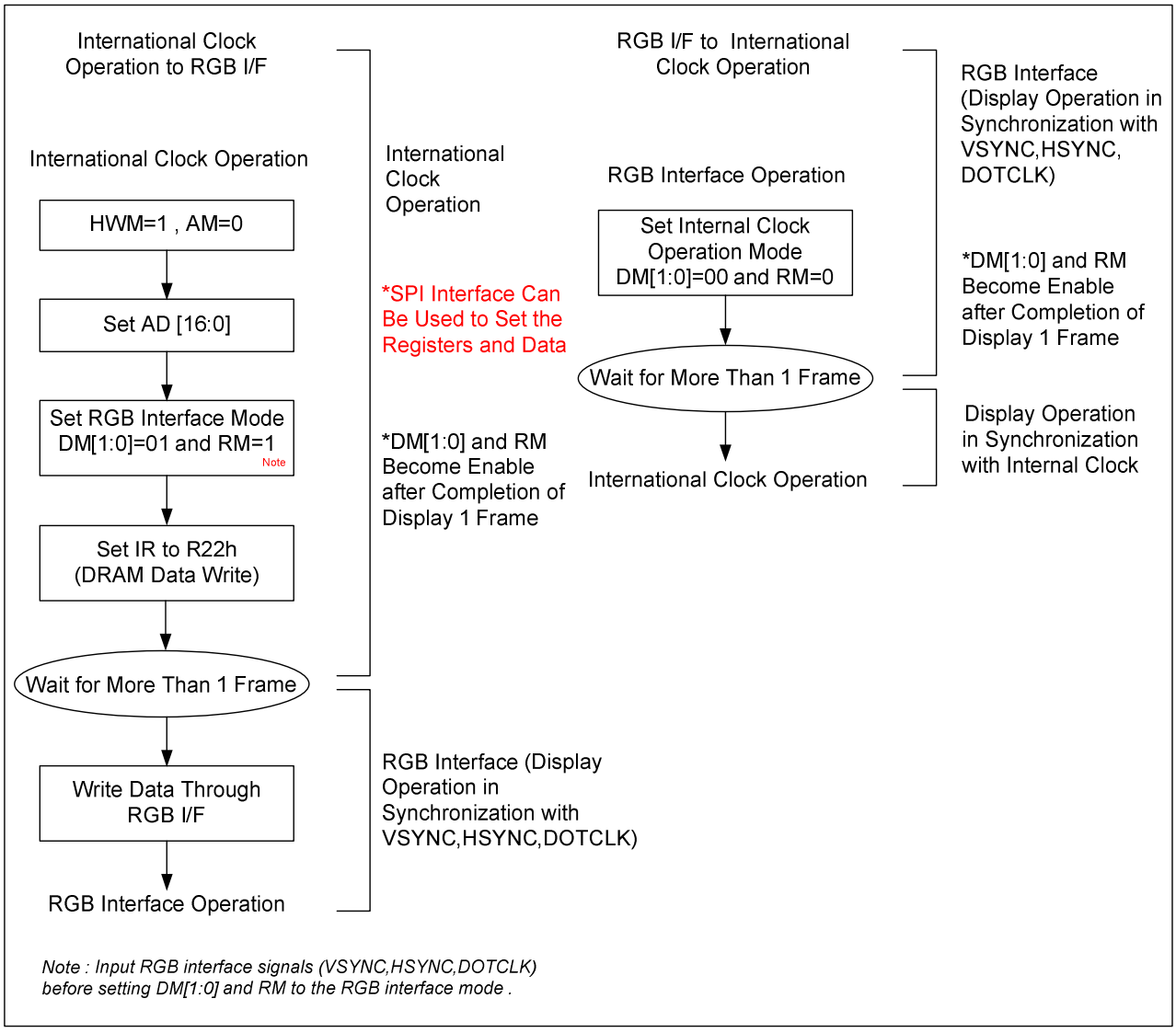


Figure 28 Internal clock operation/RGB interface mode switching

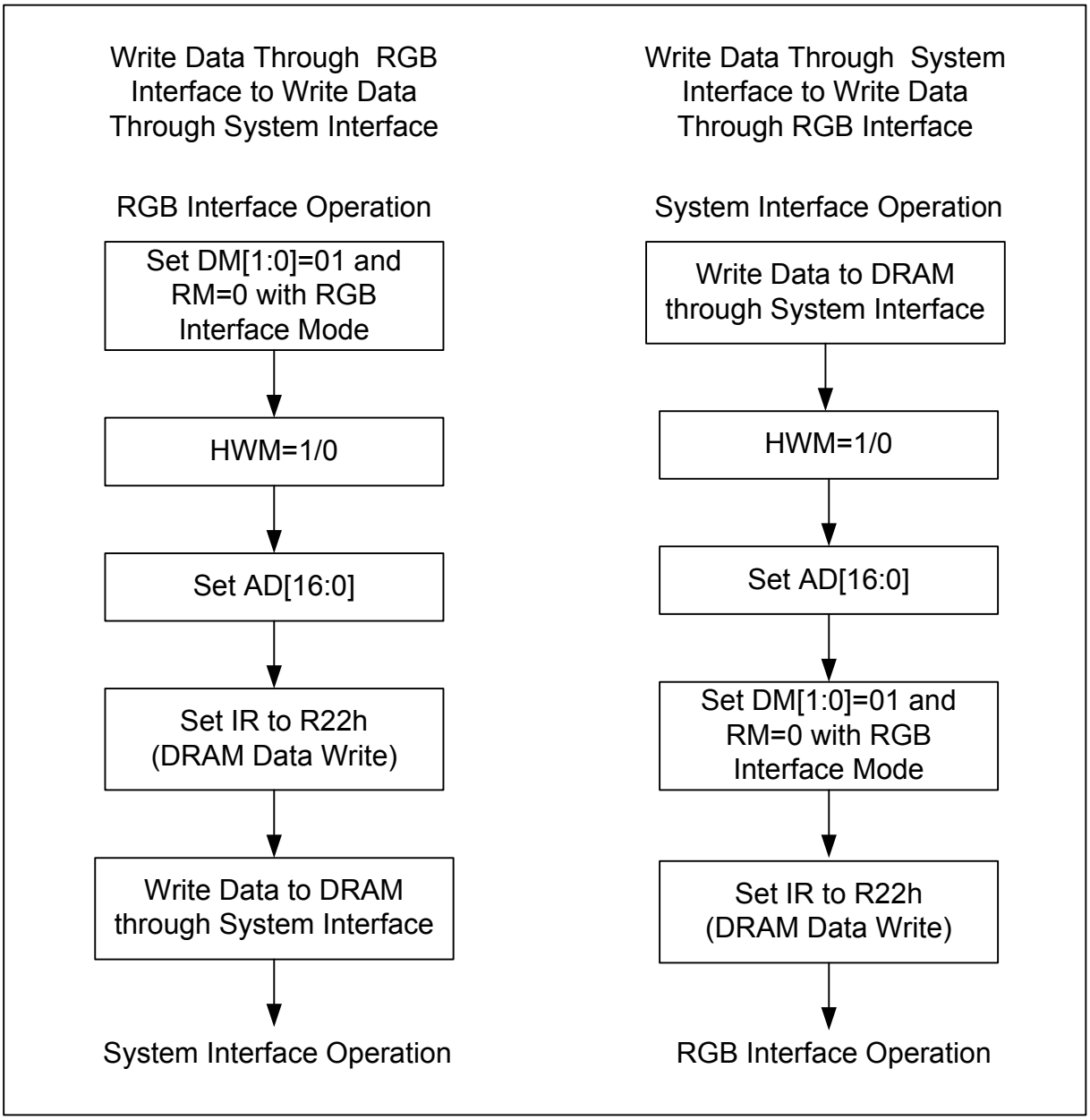


Figure 29 DRAM access between system interface and RGB interface

8.4.. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “010x” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND.

The SPI interface operation enables from the falling edge of CSX and ends of data transfer on the rising edge of CSX. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ST7781R.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, ST7781R starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ST7781R are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

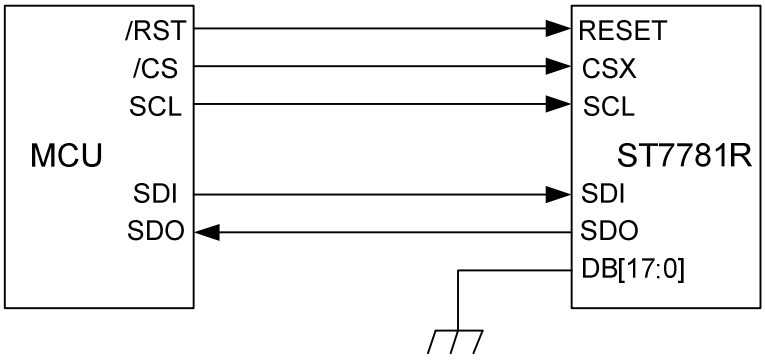
Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device IC Code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

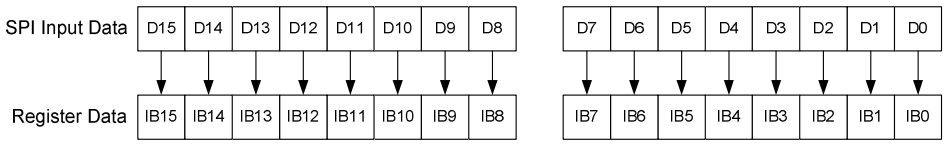
Notes: .ID bit is selected by setting the IM0/ID pin

RS and R/W Bit Function

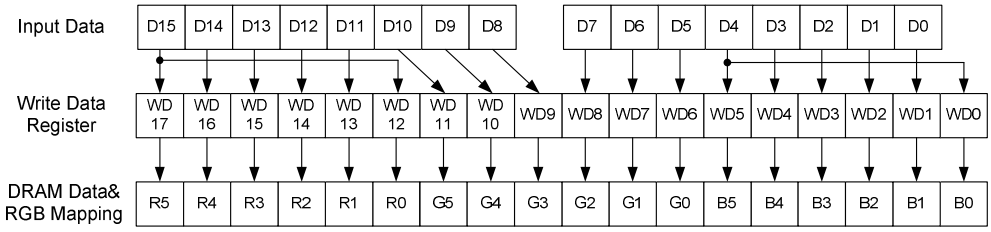
RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or DRAM data
1	1	Read a register or DRAM data



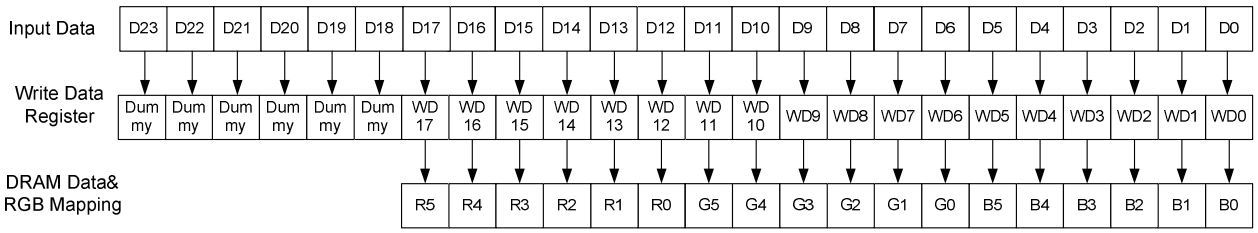
Serial Peripheral Interface for register access



Serial Peripheral Interface 65K colors



Serial Peripheral Interface 262K colors (TRI=1,DFM=0)



Serial Peripheral Interface 262K colors (TRI=1,DFM=1)

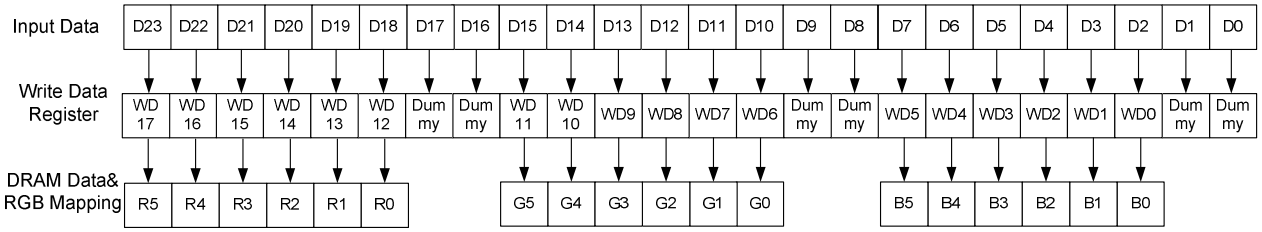


Figure 30 Data Format of SPI Interface

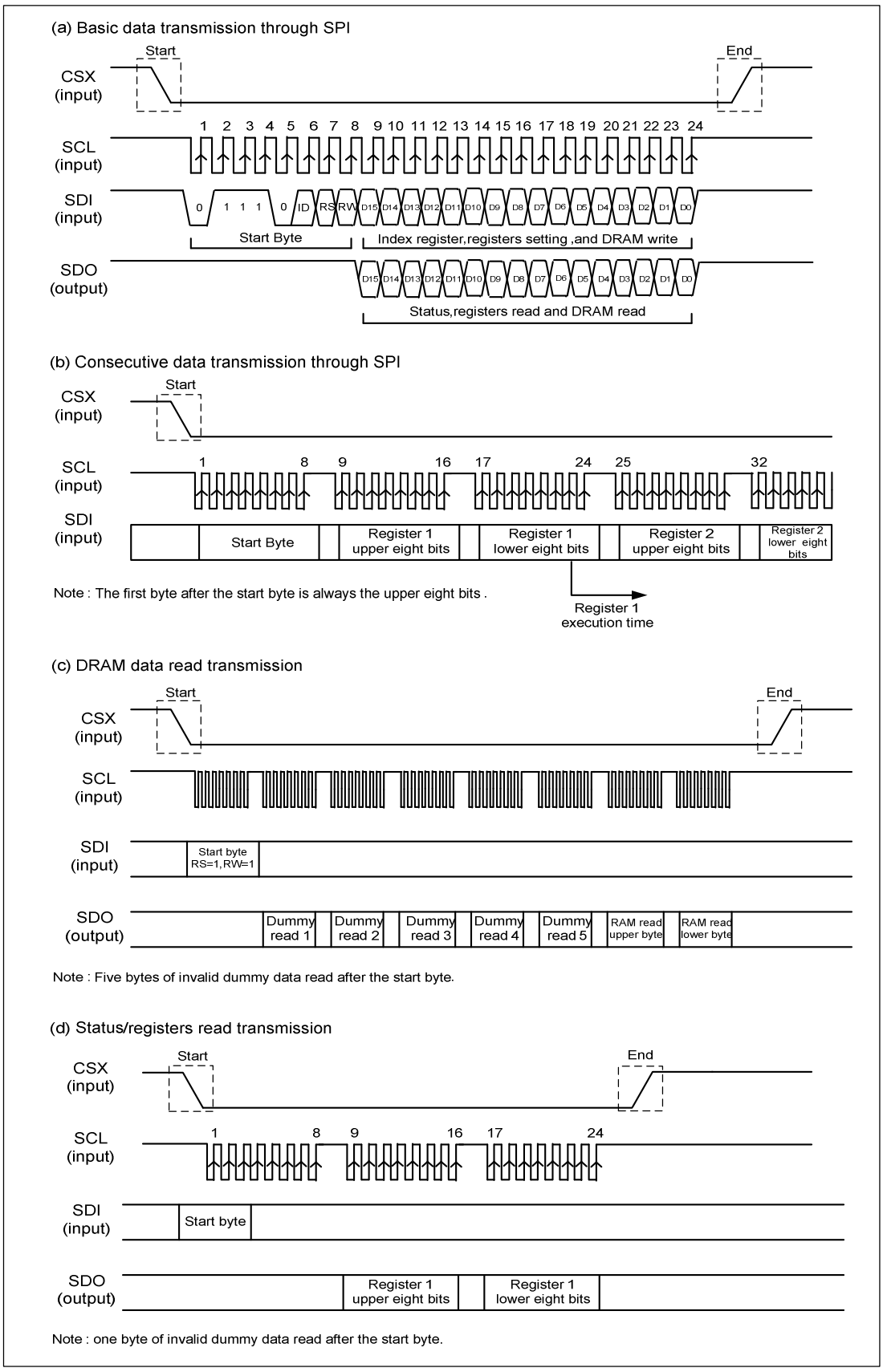
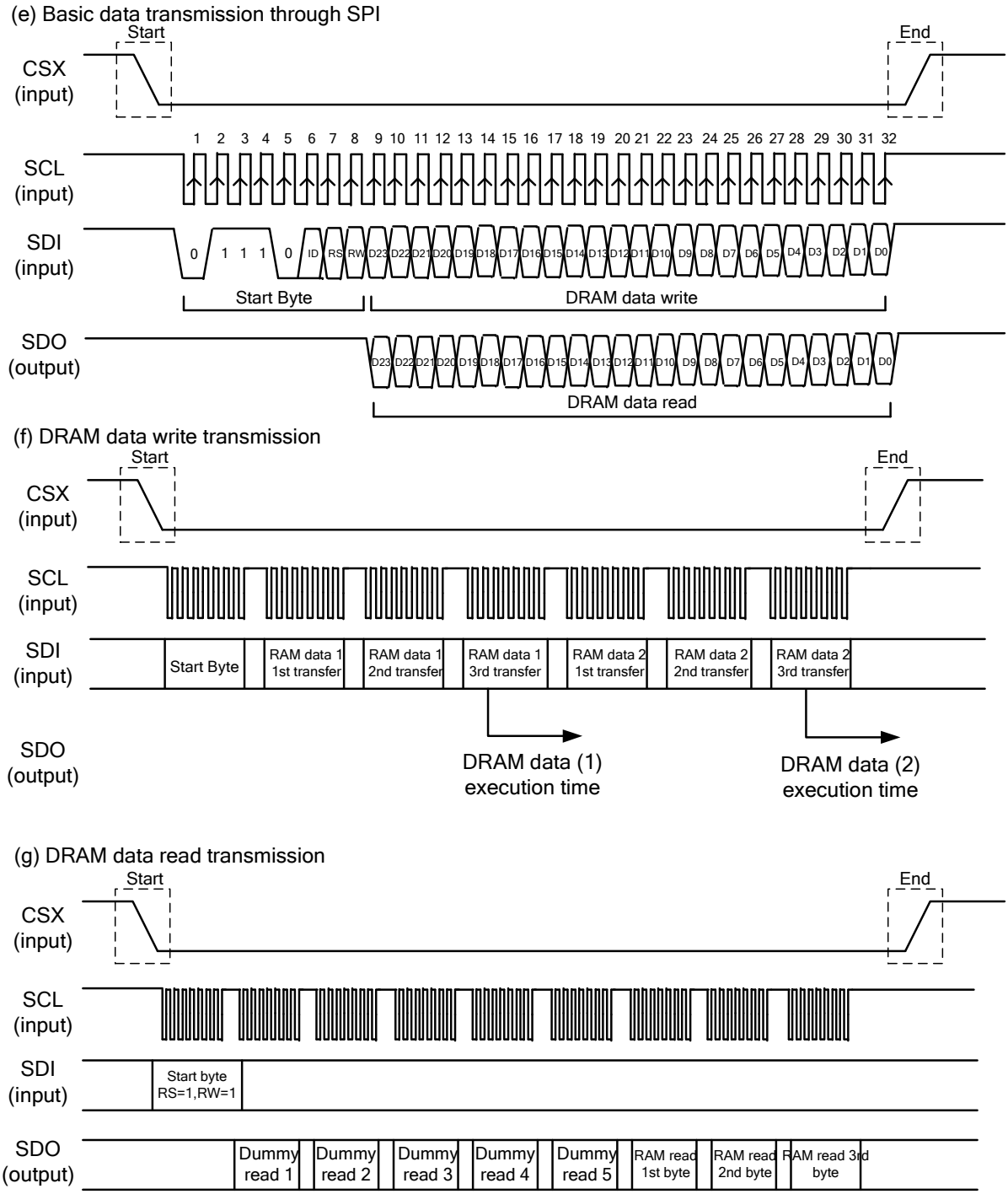


Figure 31 Data transmission through serial peripheral interface (SPI)



Note : Five bytes of invalid dummy data read after the start byte.

RAM data transfer in SPI mode when TRI = 1 and DFM = 1 or 0

Figure 32 Data transmission through serial peripheral interface (SPI, TRI="1" and DFM="1 or 0")

8.5.. VSYNC Interface

8.5.1 18-bit RGB Interface

The ST7781R incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

When DM[1:0]=”10” and RM=”0”, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables tearing-free display of motion pictures with the conventional interface.

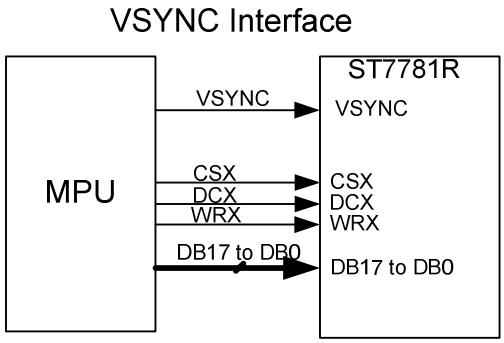


Figure 33 Data transmission through VSYNC interface

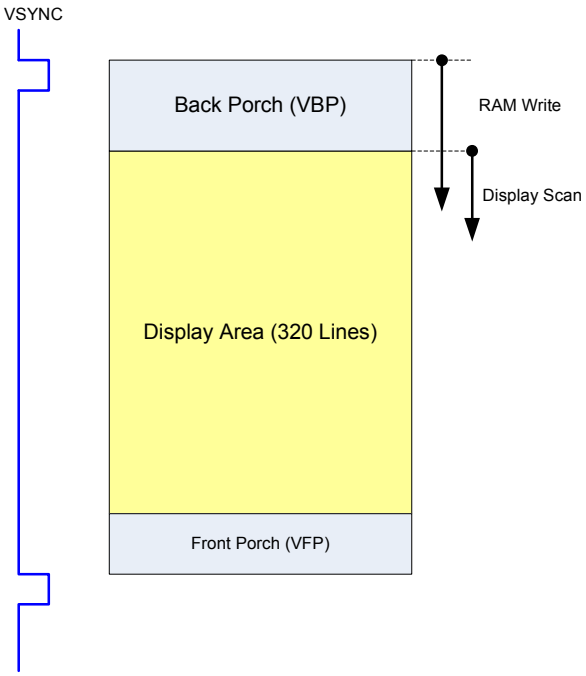


Figure 34 Operation through VSYNC Interface

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

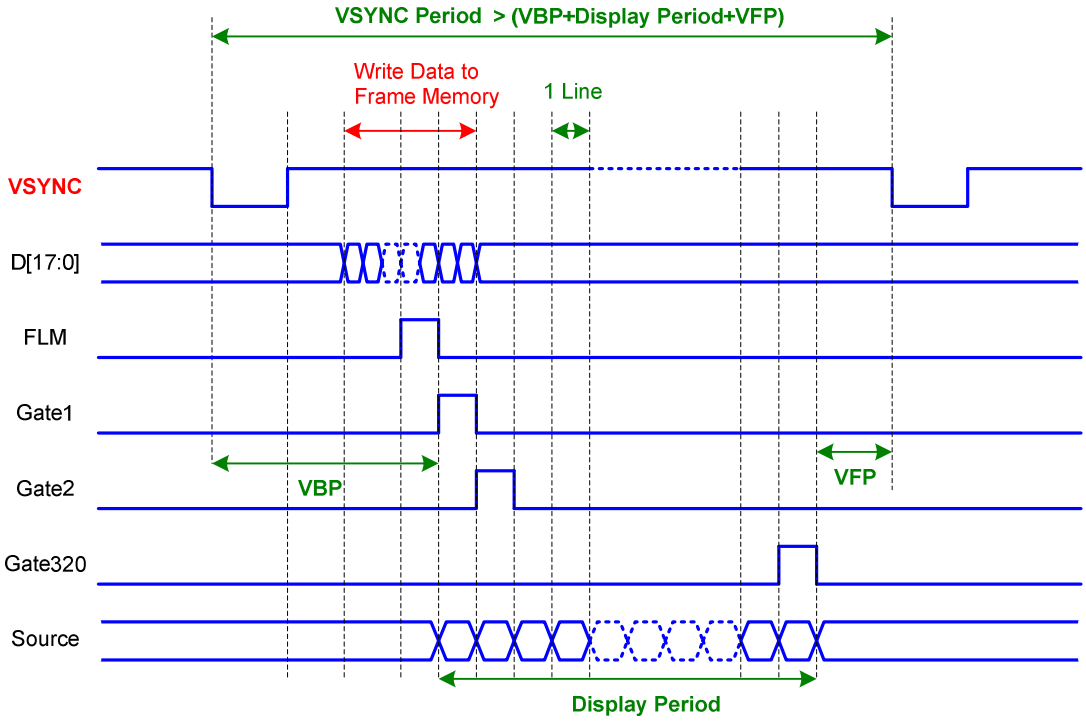


Figure 35 Timing Diagram of VSYNC Interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below. The internal memory writing address counter is reset by VSYNC. So, insure interval time between VSYNC falling and DRAM data writing.

Note:

1. VSYNC period should always be constant. If not, some degradation of display such as flicker may occur in LCD system.

2. Display data don't need to be written for every VSYNC period. For example, any system is working under 60Hz frame rate and 30-fps motion picture condition. So being written display data for every other frame would be enough.

8.5.2 VSYNC Interface Mode

8.5.2.1 Leading Mode

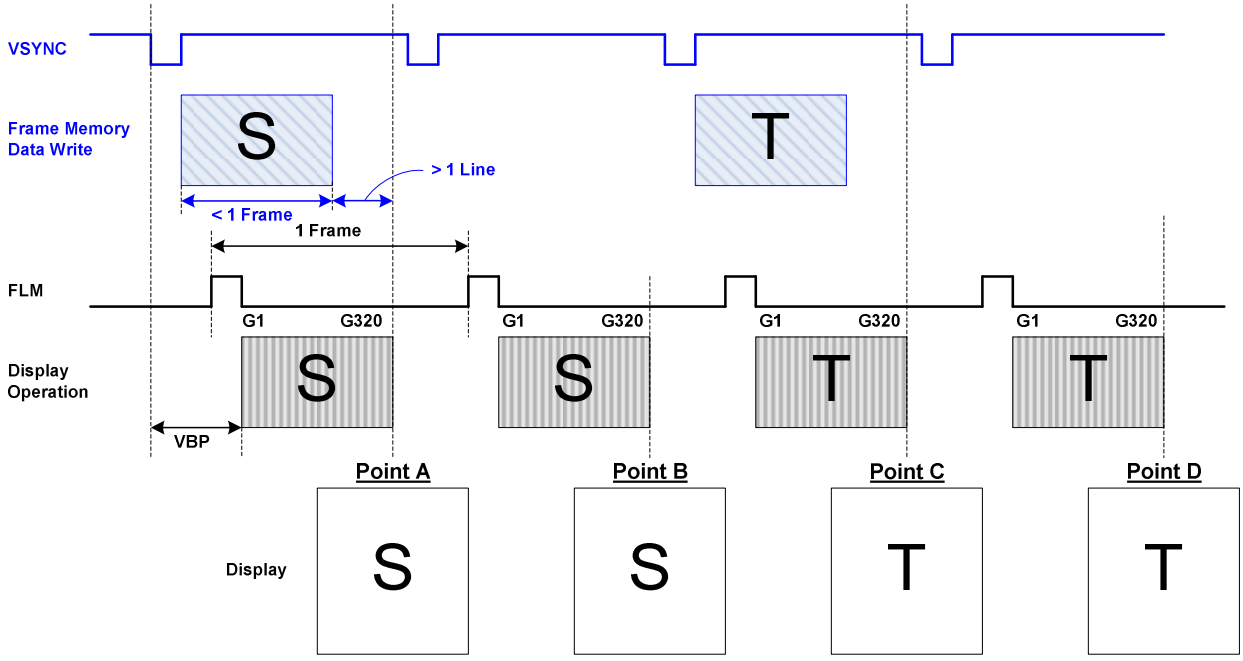


Figure 36 Operation for Leading Mode of VSYNC Interface

8.5.2.2 Lagging Mode

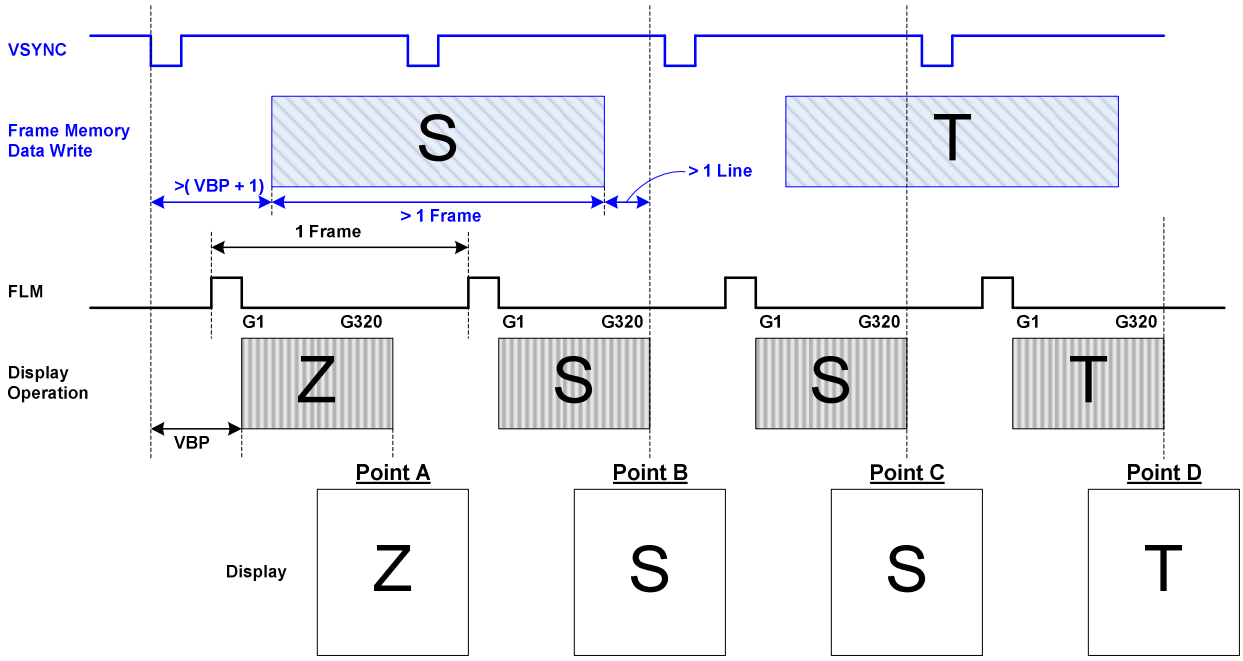


Figure 37 Operation for Lagging Mode of VSYNC Interface

Notes:

1. When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

1. The minimum DRAM write speed must be satisfied and the frequency variation must be taken into consideration.

2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.

3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.

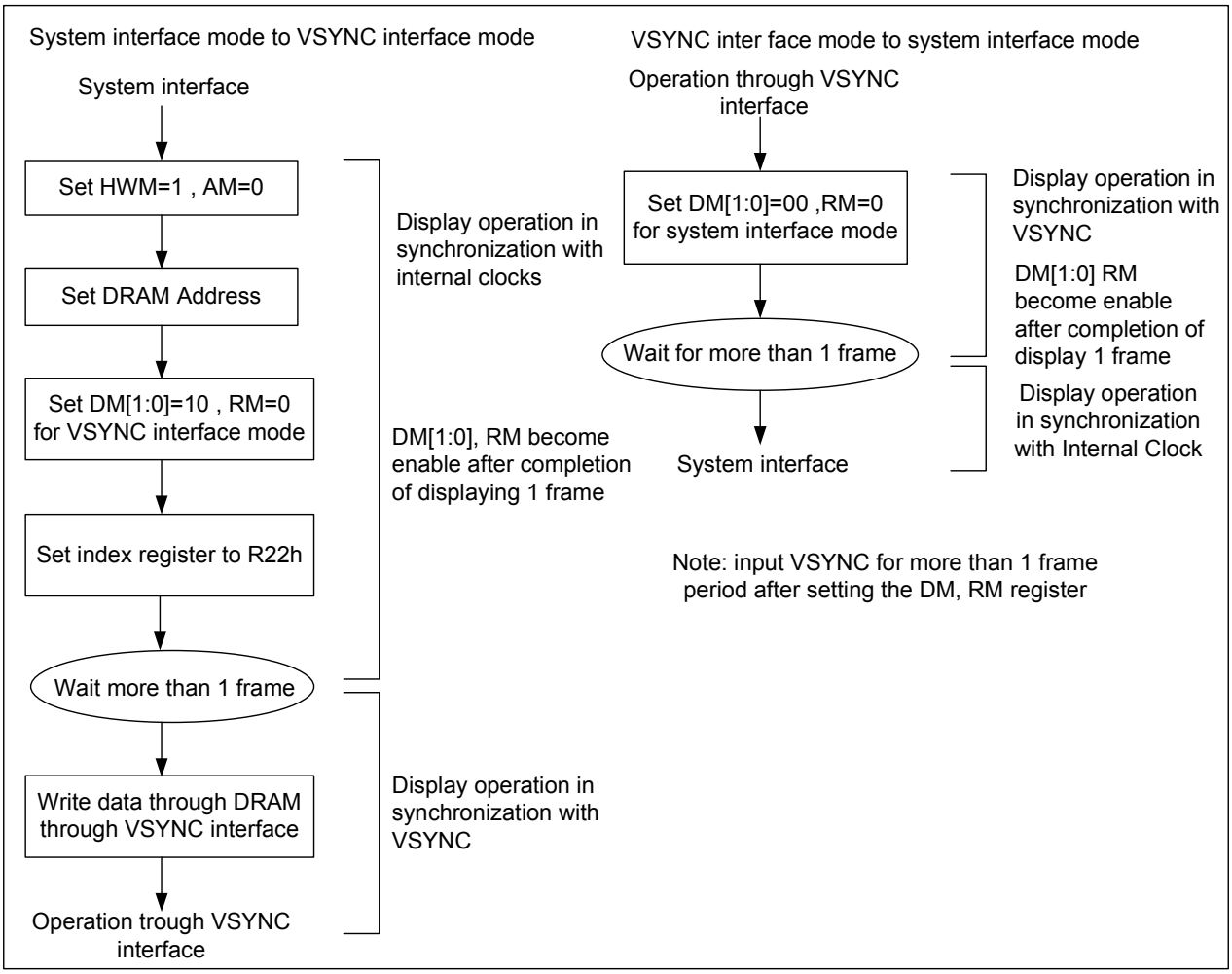


Figure 38 Transition flow between VSYNC and internal clock operation modes

8.6.. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface.

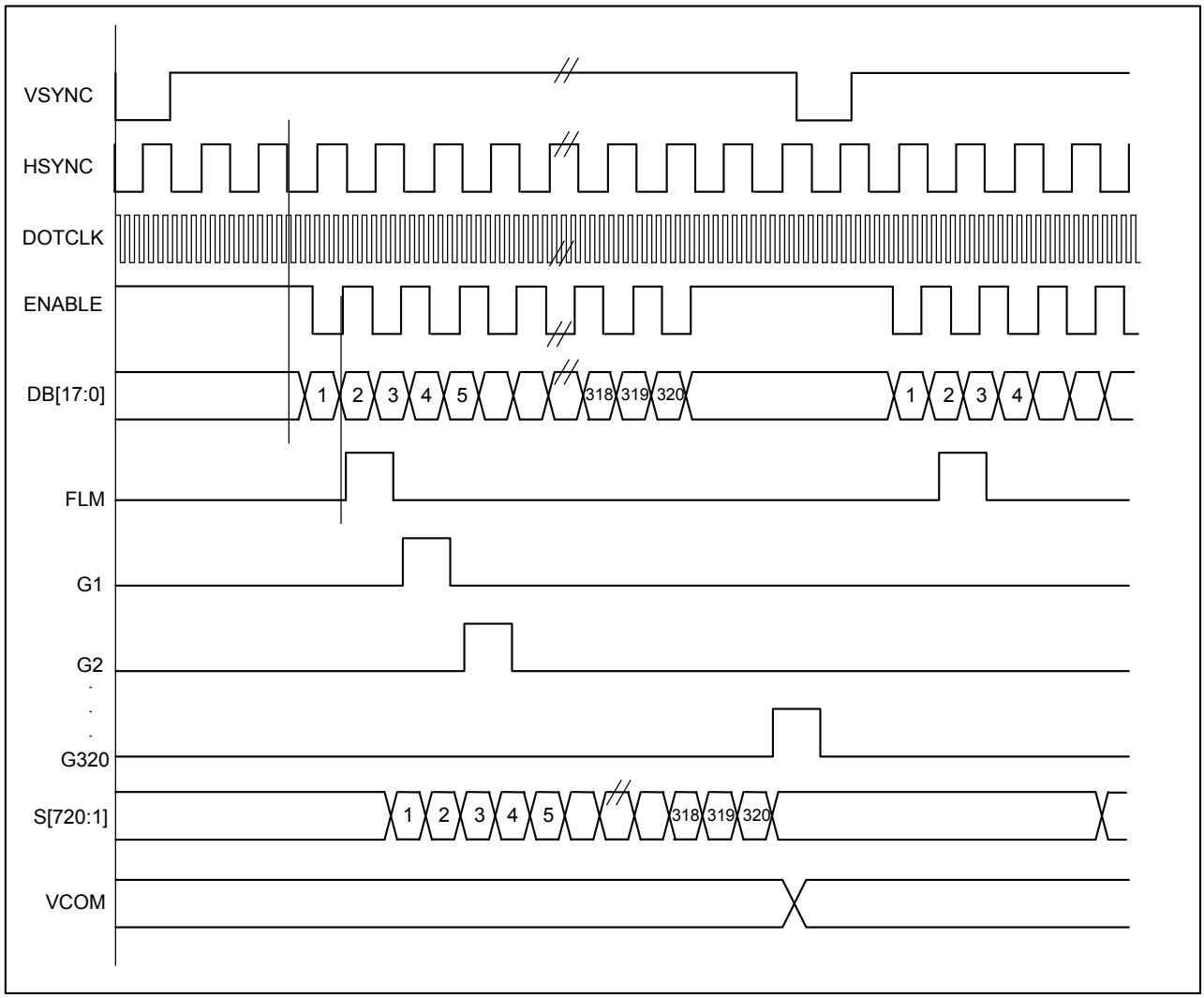


Figure 39 Relationship between RGB I/F signals and LCD Driving Signals for Panel

8.7.. Register Descriptions

ST7781R adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional Blocks of ST7781R starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and Display data will be written. The register selection signal (RS), the read/write signals (RDX/WRX) and data bus D[17:0] are used to read/write the instructions and data of ST7781R. The registers of the ST7781R are categorized into the following groups.

1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal DRAM address (AC)
7. Transfer data to/from the internal DRAM (R22)
8. Internal grayscale γ-correction (R30 ~ R39)

Normally, the display data (DRAM) is most often updated, and in order since the ST7781R can update internal DRAM address automatically as it writes data to the internal DRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. The way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

Serial Peripheral Interface for register access

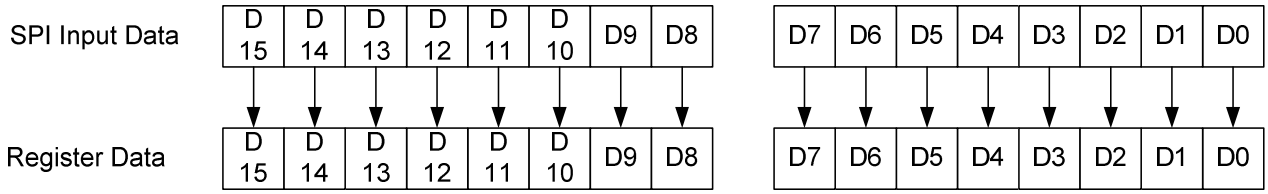
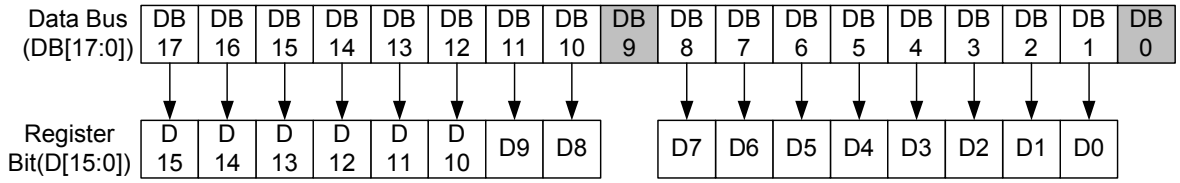
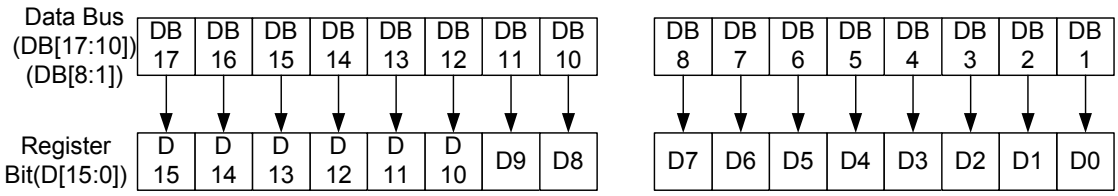


Figure 40 Register Setting with Serial Peripheral Interface (SPI)

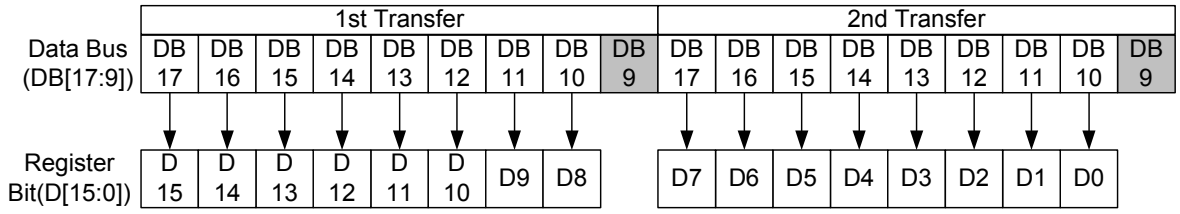
i80-18bits Data bus Interface



i80-16bits Data bus Interface



i80-9bits Data bus Interface



i80-8bits Data bus Interface / Serial Peripheral Interface (2/3 transmission)

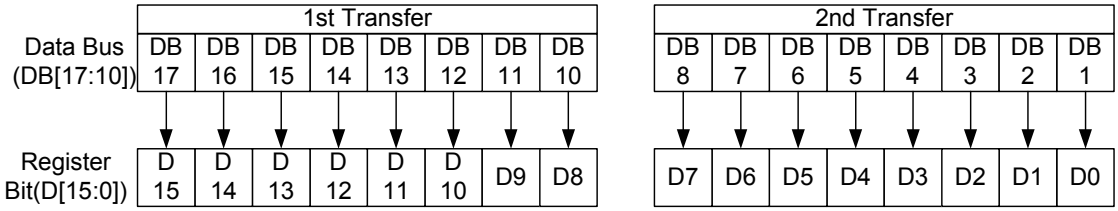
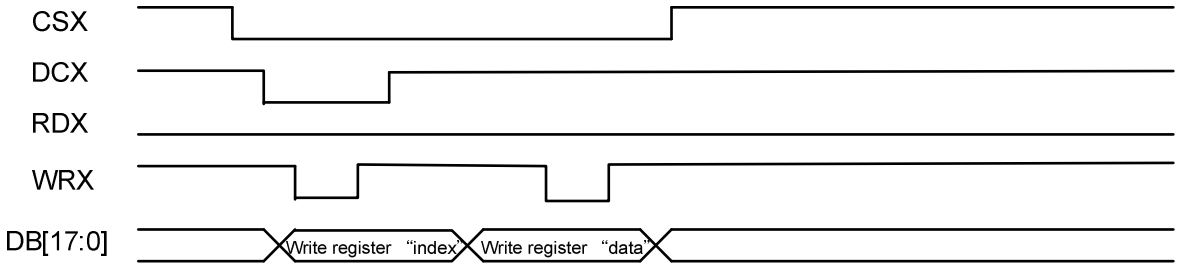


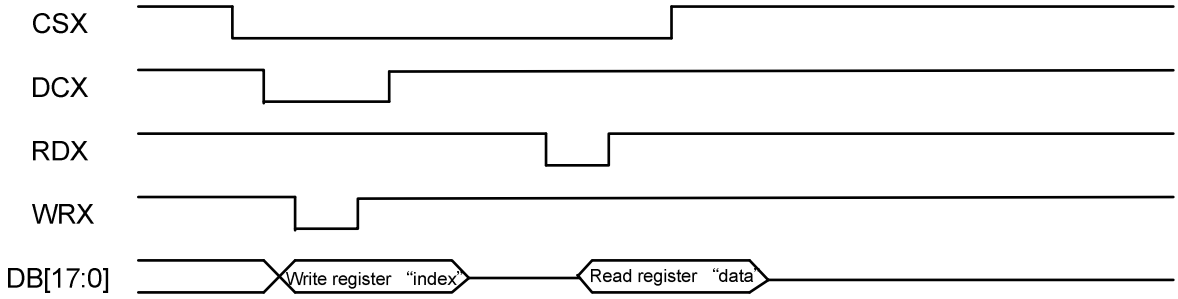
Figure 41 Register setting with i80 System Interface

i80 18-/16-bit System Bus Interface Timing

(a) Write to register

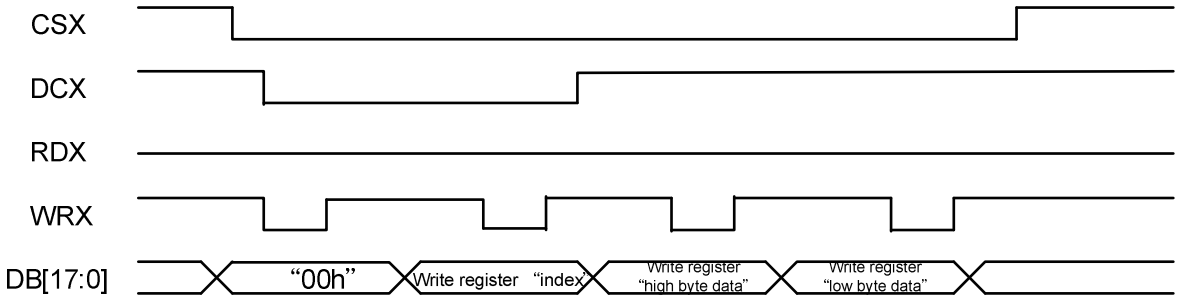


(b) Read from register



i80 9-/8-bit System Bus Interface Timing

(a) Write to register



(b) Read from register

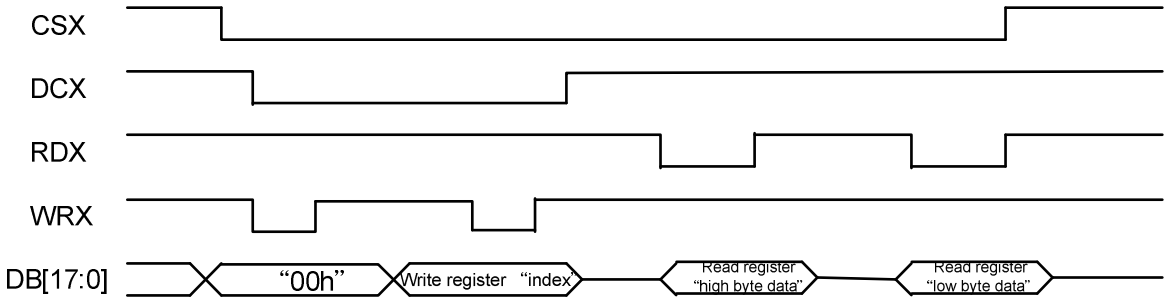


Figure 42 Register Read/Write Timing of i80 System Interface

9 COMMAND

9.1.. System Function Command List

No	Registers	W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	R	1	0	1	1	1	0	1	1	1	1	0	0	0	0	0	1	1
01h	Driver Output Control	W/R	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
03h	Entry Mode	W/R	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0
04h	Resize Control	W/R	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
07h	Display Control 1	W/R	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display control 2	W/R	1	0	FP6	FP5	FP4	FP3	FP2	FP1	FP0	0	BP6	BP5	BP4	BP3	BP2	BP1	BP0
09h	Display Control 3	W/R	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W/R	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Marker Position	W/R	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W/R	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	DPL	EPL
10h	Power Control 1	W/R	1	0	0	0	SAP	0	0	0	0	APE	AP2	AP1	AP0	0	**DSTB**	SLP	STB
20h	Horizontal DRAM Address Set	W/R	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical DRAM Address Set	W/R	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	DRAM Write Data (WD17-0) / Read Data (RD17-0)															
22h	Read Data from GRAM	R	1																
30h	Gamma Control 1	W/R	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W/R	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W/R	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W/R	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]
36h	Gamma Control 5	W/R	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W/R	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W/R	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W/R	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W/R	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]
3Dh	Gamma Control 10	W/R	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W/R	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W/R	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W/R	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W/R	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W/R	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

61h	Base Image Display Control	W/R	1	h	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W/R	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W/R	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W/R	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W/R	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W/R	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W/R	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W/R	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W/R	1	0	0	0	0	0	0	DIVI1	DIVI0	0	RTNI6	RTNI5	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
95h	Panel Interface Control 2	W/R	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
B0h	Power Control 2	W/R	1	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VGLSEL1	VGLSEL0	1	1	VGHBT1	VGHBT0
B1h	Power Control 3	W/R	1	0	0	0	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	0	0	0	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0
B2h	Power Control 4	W/R	1	0	0	0	0	0	AVCLS2	AVCLS1	AVCLS0	0	0	BCLK_DIV1	BCLK_DIV0	0	AVDDS2	AVDDS1	AVDDS0
B3h	Power Control 5	W/R	1	0	0	0	0	DC11	DC10	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
B5h	Power Control 6	W/R	1	0	0	0	0	0	0	MODE1	MODE0	OSAP2	OSAP1	OSAP0	0	0	0	0	0
B6h	Power Control 7	W/R	1	0	0	0	0	0	0	0	0	NO1	NO0	0	0	SDT1	SDT0	0	0
D2h	NVM ID Code	W/R	1	0	0	0	0	0	0	0	0	0	ID6	ID5	ID4	ID3	ID2	ID1	ID0
D9h	NVM Control Status	W/R	1	0	0	0	0	0	0	0	0	0	VMF_EN	0	0	0	0	0	0
DFh	NVM Write Command	W	1	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1
FAh	NVM Enable	W/R	1	0	0	0	0	0	0	0	0	PROG_MODE	0	0	0	0	1	MTP_PROG	0
FEh	NVM VCOM Offset	W/R	1	0	0	0	0	0	0	0	0	1	0	0	VMF4	VMF3	VMF2	VMF1	VMF0
FFh	NVM Command Enable	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CMD2_EN

Table 9 System Function Command List

9.2.. System Function Command

9.2.1 Index (IR)

Note: "-"Don't care

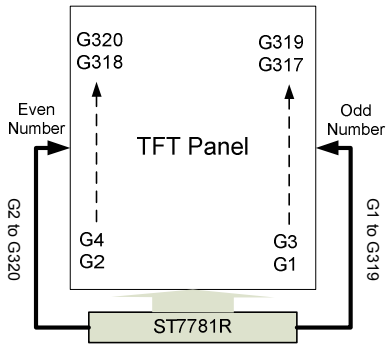
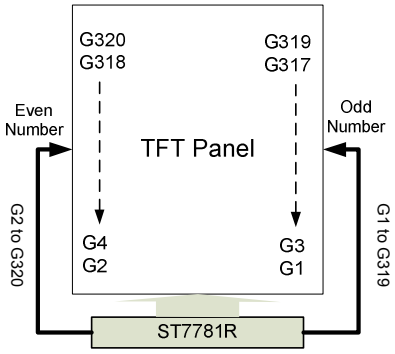
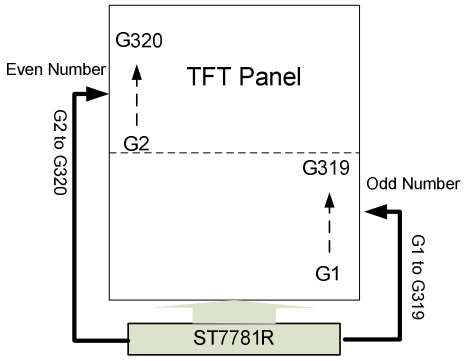
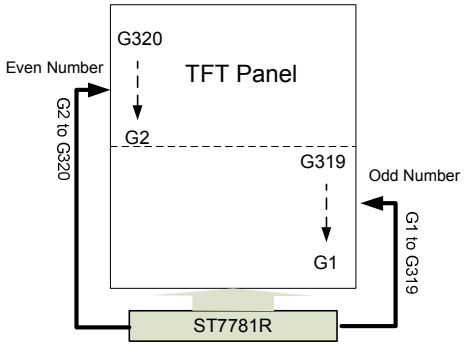
Index(IR)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	↑	1	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Description	The index register specifies the index R00h to RFFh of the control register or RAM control to be accessed. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.																	

9.2.2 Device ID Code Read (R00h)

Device ID Code Read Out (R00h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	1	↑	0	1	1	1	0	1	1	1	1	0	0	0	0	0	1	1
Description	When read this register, the device output device ID code																	

9.2.3 Device Output Control (R01h)

Device Output Control (R01H)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description	**SS**: Select the shift direction of outputs from the source driver. When SS = 0, the shift direction of outputs is from S1 to S720 When SS = 1, the shift direction of outputs is from S720 to S1. In addition to the shift direction, the settings for both SS and BGR bits are required to change the Assignment of R, G, B dots to the source driver pins. To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0. To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1. *Note: When changing SS or BGR bits, DRAM data must be rewritten.* **SM**: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.																

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1,G2,G3,G4…..,G316 G317,G318,G319, G320
0	1		G320,G319,……..G316 G7,G6,G5,G4,G3,G2,G1
1	0		G1,G3,G5…….G311 G313,G315,G317,G319 G2,G4,G6…….G312 G314,G316,G318,G320
1	1		G320,G318,……..G14 G12,G10,G8,G6,G4,G2 G319,G317……..G13 G11,G9,G7,G5,G3,G1

9.2.4 Entry Mode (R03h)

Entry Mode (R03h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0
Default value			0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Description

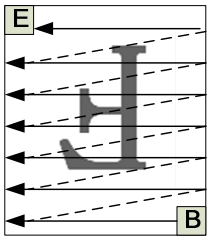
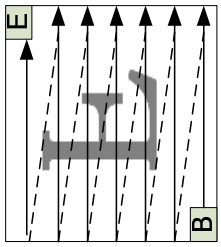
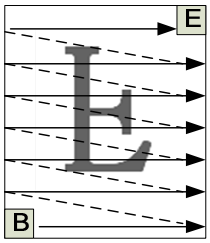
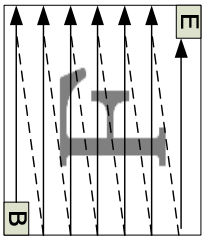
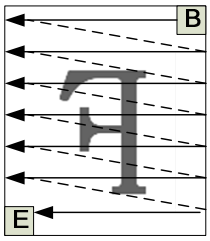
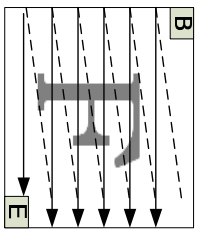
AM: Sets the DRAM Update Direction

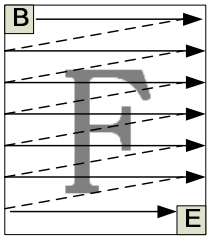
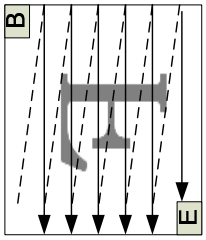
When AM = “0”, set the horizontal writing direction.

When AM = “1”, set the vertical writing direction.

When a window area is set by registers R50h ~R53h, only the addressed DRAM area is updated based on I/D [1:0] and AM bits setting.

I/D [1:0]: Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data.

AM	ID[1:0]	Write DRAM Direction	AM	ID[1:0]	Write DRAM Direction
0	00		1	00	
0	01		1	01	
0	10		1	10	

0	11		1	11	

ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = “0”: The origin address is not moved. In this case, specify the address to start write operation according to the DRAM address map within the window address area.
ORG = “1”: The original address “00000h” moves according to the I/D[1:0] setting.

Notes 1: When ORG=1, only the origin address address”00000h” can be set in the RAM address set registers R20h, and R21h.

Notes2: In RAM read operation, make sure to set ORG=0.

HWM: The ST7781R writes data in high speed with low power consumption by setting HWM = 1. The data to be written within the window address area is buffered in order to write the data in units of horizontal lines. This can minimize the Number of RAM access and the power consumption required in data write operation.

When HWM = 1, make sure to set AM = 0 (horizontal direction) and write the data in each horizontal line of the window address area at a time. If the data is not enough to rewrite the horizontal line of the window address area, the DRAM data in that line is not overwritten.

Notes1: The ST7781R requires no dummy write operation in high-speed write operation.

Notes2: When terminating DRAM data write operation in the middle of the line and executing another instruction, the data in the buffer is cleared.

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the DRAM.
BGR = 0: Write data in the order of RGB to the DRAM.

BGR=0																	
D17	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

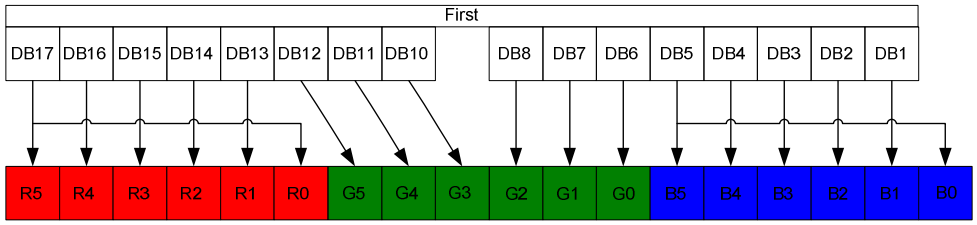
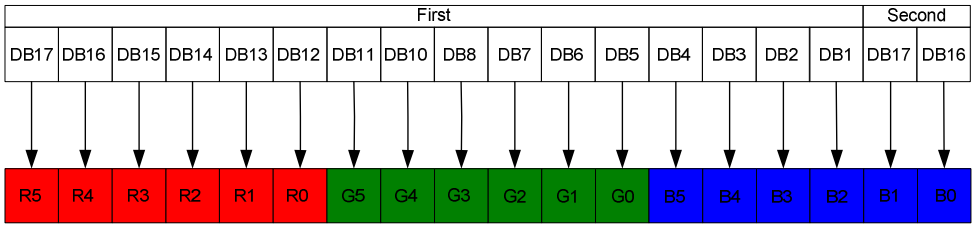
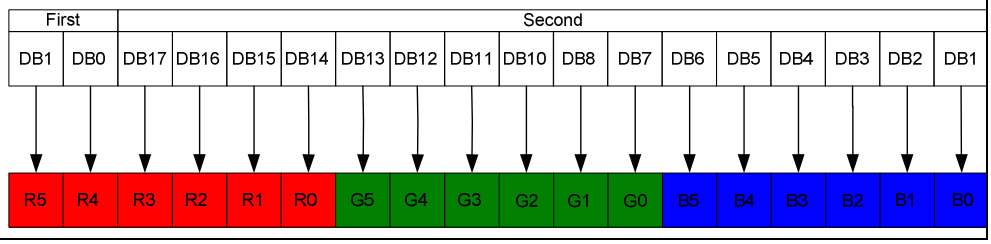
BGR = 1: Reverse the order from RGB to BGR in writing data to the DRAM.

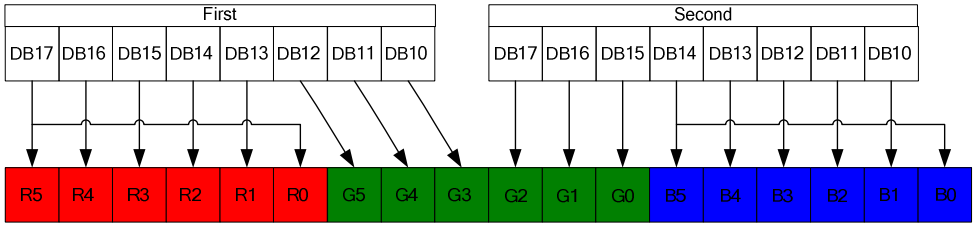
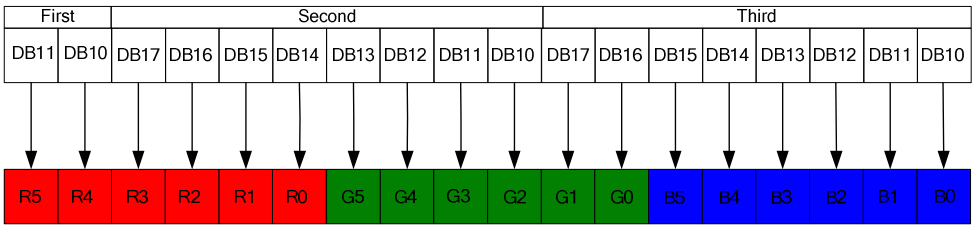
BGR=1

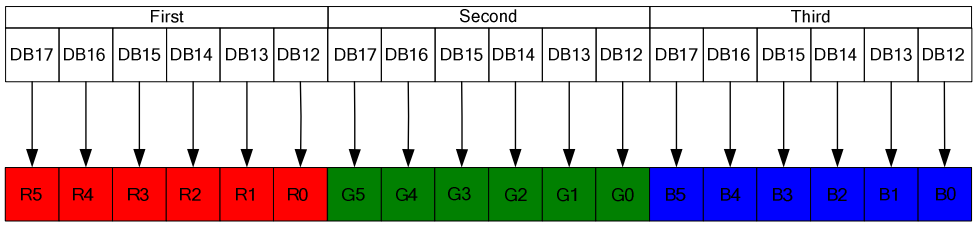
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
]	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

TRI: When TRI = “1”, data are transferred to the internal DRAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = “0”.

DFM: Set the mode of transferring data to the internal RAM when TRI = “1”.

TRI	DFM	8080-16bits Interface Color Format
0	*	
1	0	
1	1	

TRI	DFM	8080-8bits Interface Color Format
0	*	
1	0	

	1	1	 First Second Third DB17 DB16 DB15 DB14 DB13 DB12 DB17 DB16 DB15 DB14 DB13 DB12 DB17 DB16 DB15 DB14 DB13 DB12 R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0

9.2.5 Resizing Control (R04h)

Resizing Control (R04h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

RSZ [1:0]: Sets the resizing factor. When the RSZ [1:0] are set for resizing, the ST7781R writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions contracted according to the factor.

RSZ1	RSZ0	Resizing Scale
0	0	No Resizing (X1)
0	1	X 1/2
1	0	Setting Inhibited
1	1	X1/4

RCH [1:0]: Sets the number of pixels made as the remainder in horizontal direction when resizing a picture. By specifying the number of remainder pixels with RCH [1:0] the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH [1:0] = “00” when not using the resizing function (RCH [1:0]=”00”) or there are no remainder pixels.

RCH1	RCH0	Number of Remainder Pixels in Horizontal Direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixel
1	1	3 Pixel

RCV [1:0]: Sets the number of pixels made as the remainder in vertical direction when resizing a picture. By specifying the number of remainder pixels with the RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV [1:0] =”00 “when not using the resizing function RCV [1:0] =”00 “or there are no remainder pixels.

RCV1	RCV0	Number of Remainder Pixels in Vertical Direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixel
1	1	3 Pixel

9.2.6 Display Control 1 (R07h)

Display Control 1 (R07h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
Default value			0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Description

D [1:0]: A graphics display is turned on the screen when writing D1 = "1", and is turned off when writing D1 = "0". When writing D1 = "0", the graphics display data is retained in the internal DRAM and the ST7781R displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D [1:0] =00, the ST7781R's internal display operation is halted completely. In combination with the GON setting, the D [1:0] setting controls display ON/OFF.

D1	D0	BASEE	Source, VCOM Output	Internal Operation
0	0	0	GND	Halt
0	1	1	GND	Operate
1	0	0	Non-lit display	Operate
1	1	0	Non-lit display	Operate
1	1	1	Base Image display	Operate

Note1: Data write operation from the microcontroller is performed irrespective of the setting of D [1:0] bits.

Note2: The D [1:0] setting is valid on both 1st and 2nd displays.

Note3: The non-lit display level from the source output pins is determined by instruction (PTS).

CL: When CL = "1", the ST7781R halt grayscale amplifiers to display 8-color with low power consumption. When setting 8-color display mode, follow the sequence of 8-color display mode setting.

CL	Display color
0	262,144
1	8

Note: When CL = 1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

GON, DTE: The combination of GON and DTE settings set the output level form gate lines (G1 ~ G320).

GON	DTE	Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The ST7781R drives liquid crystal with non-lit display level or drives only partial image display areas.

BASEE = 1: A base image is displayed on the screen.

PTDE [1:0]: Partial image 2 and Partial image 1 enable bits

PTDE1/0 = 0: turns off partial image. Only base image is displayed.

PTDE1/0 = 1: turns on partial image.

9.2.7 Display Control 2 (R08h)

Display Control 2 (R08h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	FP6	FP5	FP4	FP3	FP2	FP1	FP0	0	BP6	BP5	BP4	BP3	BP2	BP1	BP0
Default value			0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Description

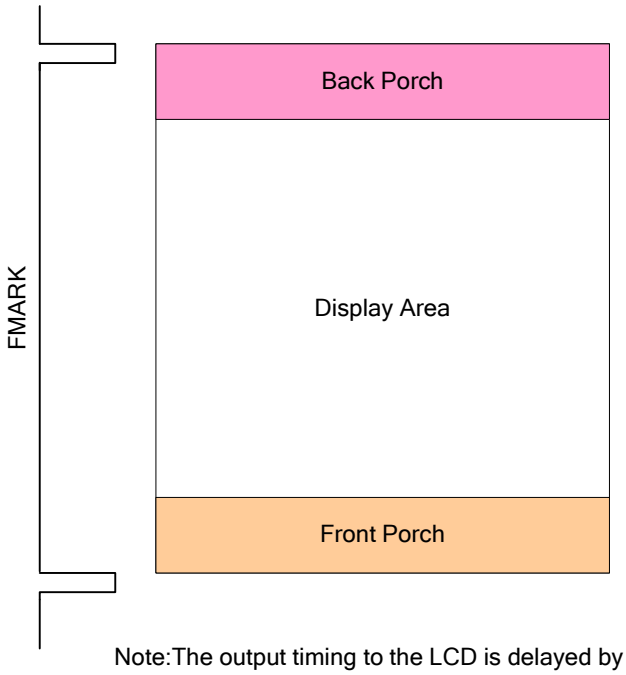
FP [6:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [6:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

Note: In 8080 interface operation mode, BP>=2 lines, FP>=2 lines

In external display interface operation, a back porch (BP) period starts on the falling edge of the FMARK signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next FMARK input is detected.

FP[6:0] BP[6:0]	Porch Lines
7'h00	Setting Prohibited
7'h01	Setting Prohibited
7'h02	2 lines
7'h03	3 lines
7'h04	4 lines
7'h05	5 lines
7'h06	6 lines
7'h07	7 lines
7'h08	8 lines
7'h09	9 lines
7'h0A	10 lines
7'h0B	11 lines
:	:
7'h7D	125 lines
7'h7E	126 lines
7'h7F	127 lines



Note:The output timing to the LCD is delayed by 2 lines period from the input FMARK signal.

9.2.8 Display Control 3 (R09h)

Display Control 3 (R09h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ICS3	ICS2	ICS1	ICS0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

PTS [1:0]: Sets the source output level in non-display area drive period.

PTS[1:0]	Source Output Level	
	Positive Polarity	Negative Polarity
00	V63P	V63N
01	V0P	V0N
10	AGND	AGND
11	Hi-Z	Hi-Z

PTG [1:0]: Sets the scan mode in non-display area. The scan mode selected by PTG [1:0] bits is applied in the non-display area when the base image is turned off and the non-display area other than the first and second partial display areas.

PTG[1:0]	Gate Output in Non-Display Area
00	Normal Scan
01	Setting Prohibited
10	Interval Scan
11	Setting Prohibited

ICS [3:0]: Set the scan cycle when PTG [1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 0 to 29. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

ICS[3:0]	Scan	$f_{FLM} = 60Hz$
0000	0 frame	-
0001	1 frame	17ms
0010	3 frame	50ms
0011	5 frame	84ms
0100	7 frame	117ms
0101	9 frame	150ms

0110	11 frame	184ms
0111	13 frame	217ms
1000	15 frame	251ms
1001	17 frame	284ms
1010	19 frame	317ms
1011	21 frame	351ms
1100	23 frame	384ms
1101	25 frame	418ms
1110	27 frame	451ms
1111	29 frame	484ms

Note1: The power efficiency improved by halting grayscale amplifiers and slowing down the step-up clock frequency can be obtained in non-display drive period.

Note2: The gate output level in non-display drive period is controlled by the PTG setting (off-scan mode).

9.2.9 Display Control 4 (R0Ah)

Display Control 4 (R0Ah)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

FMARKOE: When FMARKOE = 1, the ST7781R starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits

FMI [2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMI[2:0]	Output Interval
000	1 Frame
001	2 Frames
011	4 Frames
101	6 Frames
Others	Setting Prohibited

9.2.10 RGB Display Interface Control 1 (R0Ch)

RGB Display Interface Control 1 (R0Ch)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

ENC [2:0]: Set the RAM write cycle through the RGB interface

ENC[2:0]	RAM Write Cycle(Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

RM: Select the interface to access the RAM.

Display Status	Operation Mode	RAM Access(RM)	Display Operation Mode(DM[1:0])
Still picture	Internal clock operation	System interface(RM = 0)	Internal clock operation (DM[1:0] = 00)
Moving picture	RGB interface (1)	RGB interface(RM = 1)	RGB interface (DM[1:0] = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface(RM = 0)	RGB interface (DM[1:0] = 01)
Moving pictures	VSYNC interface	System interface(RM = 0)	VSYNC interface (DM[1:0] = 10)

Note1: Registers are set only via the system interface or SPI interface.

Note2: Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

DM [1:0]: Select the display operation mode.

DM[1:0]	Display Interface
00	Internal system clock
01	RGB interface
10	VSYNC interface
11	Setting disabled

Note1: The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RIM [1:0]: Select the RGB interface data format.

RIM[1:0]	RGB Interface Mode
00	18-bit RGB interface (1 transfer/pixel), DB[17:0]
01	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1]
10	6-bit RGB interface (3 transfers/pixel), DB[17:12]
11	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

9.2.11 Frame Marker Position (R0Dh)

Frame Marker Position (R0Dh)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

FMP [8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is output at the start of back porch period for 1H period. FMARK can be used as the trigger signal for frame synchronous write operation.

FMP[8:0]	FMARK Output Position
9'h000	0th line
9'h001	1st line
9'h002	2nd line
9'h003	3rd line
. . .	. . .
9'h174	372nd line
9'h175	373rd line
9'h176	374th line
9'h177	375th line

9.2.12 RGB Display Interface Control 2 (R0Fh)

RGB Display Interface Control (R0Fh)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description			**VSPL** : Sets the signal polarity of the VSYNC pin. VSPL=”0”, Low active VSPL=”1”, High active **HSPL** : Sets the signal polarity of the HSYNC pin. HSPL=”0”, Low active HSPL=”1”, High active **EPL** : Sets the signal polarity of the ENABLE pin. EPL = “0” The data DB17-0 is written when ENABLE = “0”. Disable data write operation when ENABLE = “1”. EPL = “1” The data DB17-0 is written when ENABLE = “1”. Disable data write operation when ENABLE = “0”. **DPL** : Sets the signal polarity of the DOTCLK pin. DPL = “0” The data is input on the positive edge of DOTCLK DPL = “1” The data is input on the negative edge of DOTCLK															

9.2.13 Power Control 1 (R10h)

Power Control 1 (R10h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	SAP	0	0	0	0	APE	AP2	AP1	AP0	0	0	SLP	STB
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

SAP: Source Driver output control

SAP="0", Source driver is disabled.

SAP="1", Source driver is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP="0", and set the SAP="1", after starting up the LCD power supply circuit.

APE: Power supply enable bit. Set APE = "1" to start generation of power supply according to the power supply startup sequence.

AP [2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0]= "000" to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Gamma Driver Amplifier	Source Driver Amplifier
000	Halt	Halt
001	1.5	1.5
010	1.25	1.25
011	1.00	1.00
100	0.75	0.75
101	0.5	0.5
110	0.25	0.25
111	Setting Prohibited	Setting Prohibited

SLP: When SLP = "1", ST7781R enters the sleep mode and the display operation stops except the RC oscillator to reduce the power consumption. No change to the DRAM data and instruction setting is accepted and he DRAM data and the instruction setting are maintained in SLP mode.

STB: When STB = "1", ST7781R enters the standby mode and the display operation stops except the DRAM power supply to reduce the power consumption. No change to the DRAM data and instruction setting is accepted and he DRAM data and the instruction setting are maintained in STB mode.

9.2.14 DRAM Horizontal/Vertical Address Set (R20h, R21h)

DRAM Horizontal/Vertical Address Set (R20h,R21h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	↑	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

AD [16:0]: A DRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the ST7781R writes data to the internal DRAM so that data can be written consecutively without resetting the address in the AC.

AD[16:0]	DRAM Data Map
17'h00000~17'h000EF	1st line DRAM Data
17'h00100~17'h001EF	2nd line DRAM Data
17'h00200~17'h002EF	3rd line DRAM Data
17'h00300~17'h003EF	4th line DRAM Data
. . .	. . .
17'h13D00~17'h13DEF	318th line DRAM Data
17'h13E00~17'h13EEF	319th line DRAM Data
17'h13F00~17'h13FFE	320h line DRAM Data

9.2.15 Write Data to DRAM (R22h)

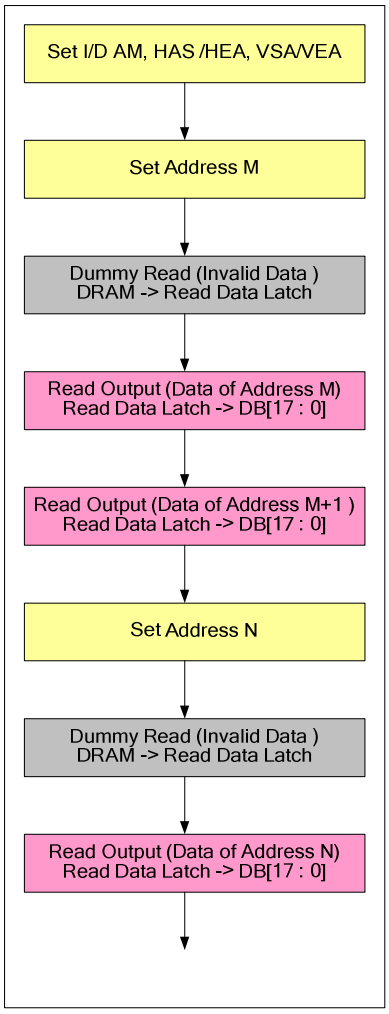
Write Data to DRAM (R22h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	WD [17:0] - DRAM Write Data															
Description			**WD [17:0]**: The ST7781R develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation. The DRAM data represents the grayscale level. The DRAM data represents the grayscale level. ST7781R automatically updates the address to the begin point according to AM and I/D[1:0] settings as it's wrote this register. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.															

9.2.16 Read Data from DRAM (R22h)

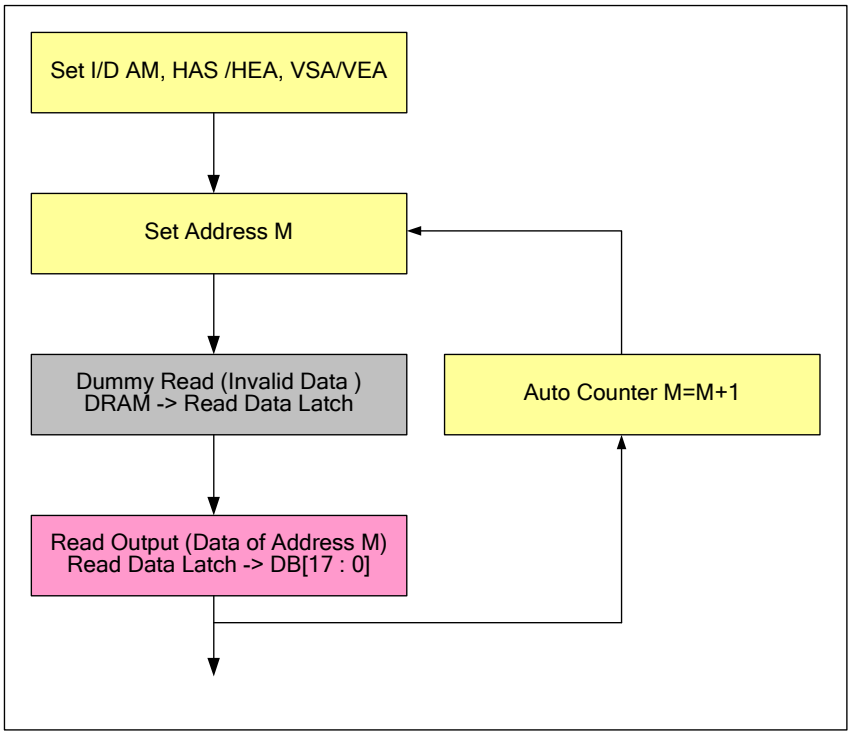
Read Data from DRAM (R22h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	1	↑	RD [17:0] - DRAM Read Data															

Description

RD [17:0]: 18-bit data read from the DRAM. RAM read data RD [17:0] is transferred via different data bus in different interface operation. When the ST7781R reads data from the DRAM to the microcomputer, the first word read immediately after RAM address set is executed is taken in the internal read-data latch and invalid data is sent to the data bus. Valid data is sent to the data bus when the ST7781R reads out the second and subsequent words. When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.



The ST7781R also support function that automatically updates the address according to AM and I/D[1:0] settings as it read data continuously address in the DRAM


Set I/D AM, HAS /HEA, VSA/VEA
Set Address M
Dummy Read (Invalid Data)
DRAM -> Read Data Latch
Auto Counter M=M+1
Read Output (Data of Address M)
Read Data Latch -> DB[17 : 0]

9.2.17 Gamma Control (R30h~R3Dh)

Gamma Control (R30h~R3Dh)																			
R30h	**RS**	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	1	↑	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31h	1	↑	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R32h	1	↑	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R35h	1	↑	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R36h	1	↑	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R37h	1	↑	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R38h	1	↑	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R39h	1	↑	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R3Ch	1	↑	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R3Dh	1	↑	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

KP5-0[2:0]: γfine Adjustment Register for Positive Polarity.

RP1-0[2:0]: γgradient Adjustment Register for Positive Polarity.

VRP1 [4:0]: γamplitude Adjustment Register for Positive Polarity.

VRP0 [3:0]: γamplitude Adjustment Register for Positive Polarity.

KN5-0[2:0]: γfine Adjustment Register for Negative Polarity.

RN1-0[2:0]: γgradient Adjustment Register for Negative Polarity.

VRN1 [4:0]: γamplitude Adjustment Register for Negative Polarity.

VRN0 [3:0]: γamplitude Adjustment Register for Negative Polarity.

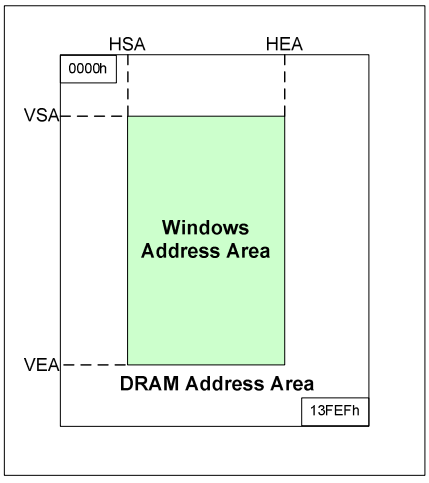
9.2.18 Horizontal and Vertical RAM Address Position (R50h, R51h, R52h, R53h)

Horizontal and Vertical RAM Address Position(R50h,R51h,R52h,R53h)																			
	RS	WRX	RDX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	1	↑	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51h	1	↑	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
Default value				0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R52h	1	↑	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53h	1	↑	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
Default value				0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

Description

HSA [7:0], HEA [7:0] HSA[7:0] and **HEA[7:0]** are the start and end addresses of the window address area in horizontal direction, respectively. HSA [7:0] and HEA [7:0] specify the horizontal range to write data. Set HSA [7:0] and HEA [7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HAS < HEA ≤ 8'hEF

VSA [8:0], VEA [8:0] VSA [8:0] and **VEA [8:0]** are the start and end addresses of the window address area in vertical direction, respectively. VSA [8:0] and VEA [8:0] specify the vertical range to write data. Set VSA [8:0] and VEA [8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h13F.



"00"h ≤HSA[7:0] ≤HEA[7:0] ≤"EF"h
"00"h ≤VSA[7:0] ≤VEA[7:0] ≤"13F"h

Note1. The window address range must be within the DRAM address space.
Note2. Data are written to DRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area.

9.2.19 Gate Scan Control (R60h, R61h, R6Ah)

Gate Scan Control (R60h,R61h)																			
R60h	**RS**	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	1	↑	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R61h	1	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6Ah	1	↑	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

When GS=0, the scan direction is from G1 to G320

When GS=1, the scan direction is from G320 to G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The DRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line	NL[5:0]	LCD Drive Line
6'h1D	240 lines	6'h23	288 lines
6'h1E	248 lines	6'h24	296 lines
6'h1F	256 lines	6'h25	304 lines
6'h20	264 lines	6'h26	312 lines
6'h21	272 lines	6'h27	320 lines
6'h22	280 lines	Others	Setting inhibited

SCN [5:0]: Specifies the gate line where the gate driver starts scan.

SCN[5:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G320	G1	G320
01h	G9	G312	G17	G304
02h	G17	G304	G33	G288
03h	G25	G296	G49	G272
04h	G33	G288	G65	G265
05h	G41	G280	G81	G240
06h	G49	G272	G97	G224

07h	G57	G264	G113	G208
08h	G65	G256	G129	G192
09h	G73	G248	G145	G176
0Ah	G81	G240	G161	G160
0Bh	G89	G232	G177	G144
0Ch	G97	G224	G193	G128
0Dh	G105	G216	G209	G112
0Eh	G113	G208	G2	G96
0Fh	G121	G200	G18	G80
10h	G129	G192	G34	G64
11h	G137	G184	G50	G48
12h	G145	G176	G66	G32
13h	G153	G168	G82	G16
14h	G161	G152	G114	G303
15h	G169	G152	G114	G303
16h	G177	G144	G130	G287
17h	G185	G136	G146	G271
18h	G193	G128	G162	G255
19h	G201	G120	G178	G239
1Ah	G209	G112	G194	G223
1Bh	G217	G104	G114	G207
1Ch	G225	G96	G130	G191
1Dh	G233	G88	G146	G175
1Eh	G241	G80	G162	G159
1Fh	G249	G72	G178	G143
20h	G257	G64	G194	G127
21h	G265	G56	G210	G111
22h	G273	G48	G226	G95
23h	G281	G40	G242	G79
24h	G289	G32	G258	G63
25h	G297	G24	G274	G47
26h	G305	G16	G290	G31
27h	G313	G8	G30	G15
28h ~ 3Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NDL: Sets the source output level in non display area. NDL bit can keep the non-display area lit on.

NDL	Non- Display Area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the ST7781R to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

REV	DRAM Data	Non- Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the ST7781R starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image Display
0	Fixed
1	Enable Scrolling

VL[8:0]: Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0] $\leqq$320.

9.2.20 Partial Image 1 Display Position (R80h)

Partial Image 1 Display Position (R80h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description			**PTDP0 [8:0]**: Sets the display start position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.															

9.2.21 Partial Image 1 Start/End Address (R81h, R82h)

Partial Image 1 Start/End Address(R81h,R82h)																		
R81h	**RS**	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	1	↑	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R82h	1	↑	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description				**PTSA0 [8:0]** and **PTEA0 [8:0]**: Sets the start line and end line addresses of the RAM area, respectively for the partial image *Note1: Make sure that PTSA0 ≤ PTEA0.*														

9.2.22 Partial Image 2 Display Position (R83h)

Partial Image 2 Display Position (R83h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description			**PTDP1 [8:0]**: Sets the display start position of partial image *Note1. The display areas of the partial images 1 and 2 must not overlap each another.*															

9.2.23 Partial Image 2 Start / End Address (R84h, R85h)

Partial Image 2 Start/End Address(R84h,R85h)																			
R84h	**RS**	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	1	↑	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R85h	1	↑	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA1	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
Default value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description				**PTSA1[8:0]** and **PTEA1[8:0]**: Sets the start line and end line addresses of the DRAM area, respectively for the partial image *Note1: Make sure that PTSA1 ≤ PTEA1.*															

9.2.24 Panel Interface Control 1 (R90h)

Panel Interface Control 1 (R90h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	DIVI1	DIVI0	0	RTNI6	RTNI5	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default value			0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Description

DIVI [1:0]: Sets the division ratio of the internal clock frequency. The ST7781R's internal operation is synchronized with the frequency divided internal clock. When DIVI[1:0] setting is changed, the width of the reference clock for liquid crystal panel control signals is changed. The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too.

DIVI[1:0]	Division Ratio	Internal Operation Clock Frequency
00	1	Fosc/1
01	2	Fosc/2
10	4	Fosc/4
11	8	Fosc/8

RTNI [6:0]: Sets 1H (line) period. This setting is enabled while the ST7781R's display operation is synchronized with internal clock.

RTNI[6:0]	Clocks/Line	RTNI[6:0]	Clocks/Line	RTNI[6:0]	Clocks/Line	RTNI[6:0]	Clocks/Line
00h	0 clock	20h	32 clocks	40h	64 clocks	60h	96 clocks
01h	1 clock	21h	33 clocks	41h	65 clocks	61h	97 clocks
02h	2 clocks	22h	34 clocks	42h	66 clocks	62h	98 clocks
03h	3 clocks	23h	35 clocks	43h	67 clocks	63h	99 clocks
04h	4 clocks	24h	36 clocks	44h	68 clocks	64h	100 clocks
05h	5 clocks	25h	37 clocks	45h	69 clocks	65h	101 clocks
06h	6 clocks	26h	38 clocks	46h	70 clocks	66h	102 clocks
07h	7 clocks	27h	39 clocks	47h	71 clocks	67h	103 clocks
08h	8 clocks	28h	40 clocks	48h	72 clocks	68h	104 clocks
09h	9 clocks	29h	41 clocks	49h	73 clocks	69h	105 clocks
0Ah	10 clocks	2Ah	42 clocks	4Ah	74 clocks	6Ah	106 clocks
0Bh	11 clocks	2Bh	43 clocks	4Bh	75 clocks	6Bh	107 clocks
0Ch	12 clocks	2Ch	44 clocks	4Ch	76 clocks	6Ch	108 clocks
0Dh	13 clocks	2Dh	45 clocks	4Dh	77 clocks	6Dh	109 clocks
0Eh	14 clocks	2Eh	46 clocks	4Eh	78 clocks	6Eh	110 clocks
0Fh	15 clocks	2Fh	47 clocks	4Fh	79 clocks	6Fh	111 clocks
10h	16 clocks	30h	48 clocks	50h	80 clocks	70h	112 clocks
11h	17 clocks	31h	49 clocks	51h	81 clocks	71h	113 clocks
12h	18 clocks	32h	50 clocks	52h	82 clocks	72h	114 clocks
13h	19 clocks	33h	51 clocks	53h	83 clocks	73h	115 clocks
14h	20 clocks	34h	52 clocks	54h	84 clocks	74h	116 clocks
15h	21 clocks	35h	53 clocks	55h	85 clocks	75h	117 clocks
16h	22 clocks	36h	54 clocks	56h	86 clocks	76h	118 clocks
17h	23 clocks	37h	55 clocks	57h	87 clocks	77h	119 clocks
18h	24 clocks	38h	56 clocks	58h	88 clocks	78h	120 clocks
19h	25 clocks	39h	57 clocks	59h	89 clocks	79h	121 clocks
1Ah	26 clocks	3Ah	58 clocks	5Ah	90 clocks	7Ah	122 clocks
1Bh	27 clocks	3Bh	59 clocks	5Bh	91 clocks	7Bh	123 clocks
1Ch	28 clocks	3Ch	60 clocks	5Ch	92 clocks	7Ch	124 clocks
1Dh	29 clocks	3Dh	61 clocks	5Dh	93 clocks	7Dh	125 clocks
1Eh	30 clocks	3Eh	62 clocks	5Eh	94 clocks	7Eh	126 clocks
1Fh	31 clocks	3Fh	63 clocks	5Fh	95 clocks	7Fh	127 clocks

9.2.25 Panel Interface Control 2 (R95h)

Panel Interface Control 2 (R95h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
Default value			0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0

Description

DIVE[1:0]: Sets the division ratio of DOTCLK when ST7781R display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	18/16-bit RGB Interface	6-bit x 3 Transfers RGB Interface
00	1/2	2 DOTCLKS	6 DOTCLKS
01	1/4	4 DOTCLKS	12 DOTCLKS
10	1/8	8 DOTCLKS	24 DOTCLKS
11	1/16	16 DOTCLKS	48 DOTCLKS

9.2.26 Power Control 2 (RB0h)

Power Control 2 (RB0h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VGLSEL1	VGLSEL0	1	1	VGHBT1	VGHBT0
Default value			0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	0

Description

VCM [5:0]: VCOM voltage setting

VCM[5:0]	VCOM	VCM[5:0]	VCOM
000000	-0.425	100000	-1.225
000001	-0.45	100001	-1.25
000010	-0.475	100010	-1.275
000011	-0.5	100011	-1.3
000100	-0.525	100100	-1.325
000101	-0.55	100101	-1.35
000110	-0.575	100110	-1.375
000111	-0.6	100111	-1.4
001000	-0.625	101000	-1.425
001001	-0.65	101001	-1.45
001010	-0.675	101010	-1.475
001011	-0.7	101011	-1.5
001100	-0.725	101100	-1.525
001101	-0.75	101101	-1.55
001110	-0.775	101110	-1.575
001111	-0.8	101111	-1.6
010000	-0.825	110000	-1.625
010001	-0.85	110001	-1.65
010010	-0.875	110010	-1.675
010011	-0.9	110011	-1.7
010100	-0.925	110100	-1.725
010101	-0.95	110101	-1.75
010110	-0.975	110110	-1.775
010111	-1	110111	-1.8
011000	-1.025	111000	-1.825
011001	-1.05	111001	-1.85
011010	-1.075	111010	-1.875
011011	-1.1	111011	-1.9

011100	-1.125	111100	-1.925
011101	-1.15	111101	-1.95
011110	-1.175	111110	-1.975
011111	-1.2	111111	-2

VGLSEL [1:0]: Set the VGL supply power level.

VGLSEL[1:0]	VGL
00	-7.5
01	-10
10	-12.5
11	-13

VGHBT [1:0]: Set the VGH supply power level.

VGHBT[1:0]	VGH
00	2*AVDD+VDD
01	3*AVDD
10	3*AVDD+VDD
11	Don’t use this setting, reserve for testing.

9.2.27 Power Control 3 (RB1h)

Power Control 3 (RB1h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	0	0	0	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0
Default value			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Description

VRHN/VRHP [4:0]: GVCL/GVDD voltage setting

VRHN[4:0]	GVCL	VRHP[4:0]	GVDD
00000	-4.7	00000	4.7
00001	-4.65	00001	4.65
00010	-4.6	00010	4.6
00011	-4.55	00011	4.55
00100	-4.5	00100	4.5
00101	-4.45	00101	4.45
00110	-4.4	00110	4.4
00111	-4.35	00111	4.35
01000	-4.3	01000	4.3
01001	-4.25	01001	4.25
01010	-4.2	01010	4.2
01011	-4.15	01011	4.15
01100	-4.1	01100	4.1
01101	-4.05	01101	4.05
01110	-4	01110	4
01111	-3.95	01111	3.95
10000	-3.9	10000	3.9
10001	-3.85	10001	3.85
10010	-3.8	10010	3.8
10011	-3.75	10011	3.75
10100	-3.7	10100	3.7
10101	-3.65	10101	3.65
10110	-3.6	10110	3.6
10111	-3.55	10111	3.55
11000	-3.5	11000	3.5
11001	-3.45	11001	3.45
11010	-3.4	11010	3.4
11011	-3.35	11011	3.35

		11100	-3.3	11100	3.3
		11101	-3.25	11101	3.25
		11110	-3.2	11110	3.2
		11111	-3.15	11111	3.15

9.2.28 Power Control 4 (RB2h)

Power Control 4 (RB2h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	AVCLS2	AVCLS1	AVCLS0	0	0	BCLK_DIV1	BCLK_DIV0	0	AVDDS2	AVDDS1	AVDDS0
Default value			0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Description

AVCLS [2:0]: AVCL voltage setting

AVCLS[2:0]	AVCL
000	-4.5
001	-4.6
010	-4.7
011	-4.8
100	-4.9
101	-5
110	-5.1
111	Don't use this setting, reserve for testing.

BCLK_DIV [1:0]: Boost pump frequency.

BCLK_DIV [1:0]	Frequency (KHz)
00	4000
01	2000
10	1333
11	1000

AVDDS [2:0]: AVDD voltage setting

AVDDS[2:0]	AVDD
000	4.5
001	4.6
010	4.7

		011	4.8
		100	4.9
		101	5
		110	5.1
		111	Don't use this setting, reserve for testing.

9.2.29 Power Control 5 (RB3h)

Power Control 5 (RB3h)																	
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	DC11	DC10	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
Default value			0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0

Description

DC [11:0]: Set the Booster circuit Step-up cycle.

DC	Step1-DC [11:10]	Step2-DC [9:8]	Step3-DC [7:6]	Step4-DC [5:4]	Step5-DC [3:2]	Step6-DC [1:0]
00	BCLK/1	BCLK/1	BCLK/1	BCLK/1	BCLK/1	BCLK/1
01	BCLK/2	BCLK/2	BCLK/2	BCLK/2	BCLK/2	BCLK/2
10	BCLK/3	BCLK/3	BCLK/3	BCLK/3	BCLK/3	BCLK/3
11	BCLK/4	BCLK/4	BCLK/4	BCLK/4	BCLK/4	BCLK/4

9.2.30 Power Control 6 (RB5h)

Power Control 6 (RB5h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	MODE1	MODE0	OSAP2	OSAP1	OSAP0	0	0	0	0	0
Default value			0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Description

Mode [1:0]

MODE[1:0]	Function
00	2X
01	2X
10	AUTO
11	3X

OSAP [2:0]: Amount of output stage current in Operational Amplifier

OSAP[2:0]	Amplifier
000	0.06
001	0.16
010	0.55
011	0.82
100	1
101	1.56
110	2.02
111	2.34

9.2.31 Power Control 7 (RB6h)

Power Control 7 (RB6h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	NO1	NO0	0	0	SDT1	SDT0	0	0
Default value			0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Description

NO [1:0]: Sets the gate output non-overlap period when the ST7781R display operation is synchronized with RGB interface signals.

NO[1:0]	Gate Non-overlap Period
00	2 clocks
01	3 clocks
10	4 clocks
11	5 clocks

SDT [1:0]: Source delay time.

SDT[1:0]	Delay time
00	2 clocks
01	4 clocks
10	6 clocks
11	8 clocks

9.2.32 NVM ID Code (RD2h)

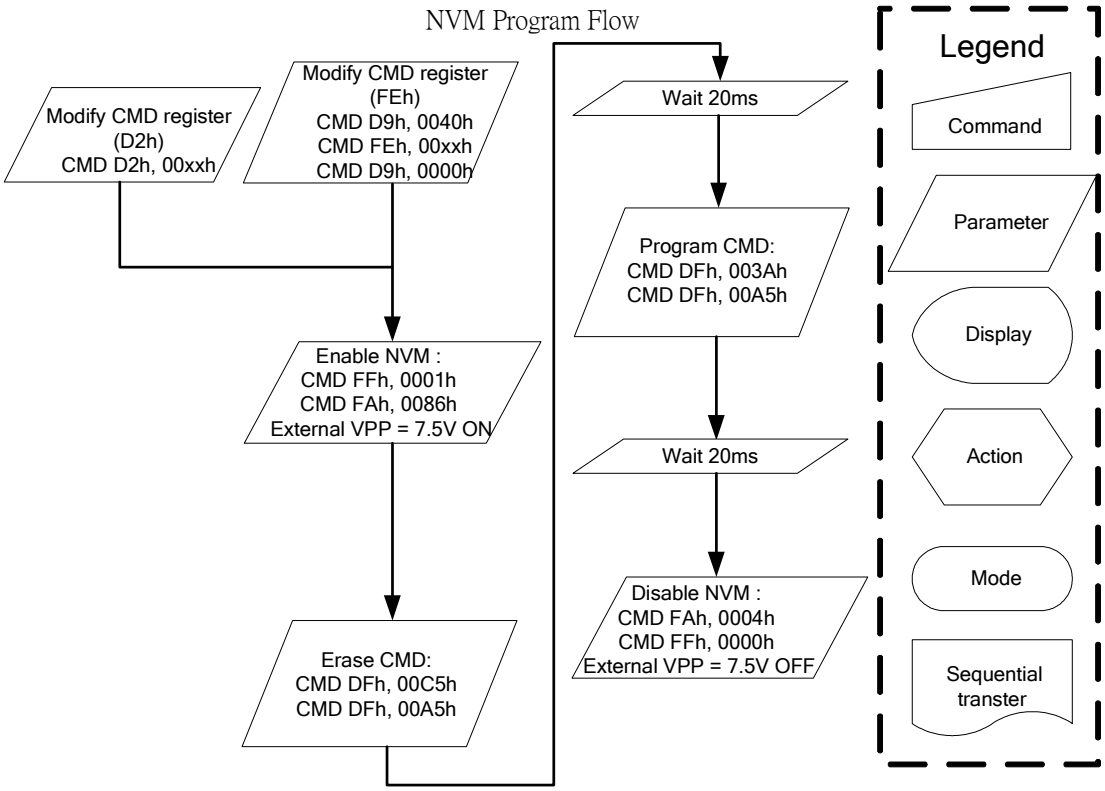
NVM ID Code (RD2h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description			**ID [6:0]**: ST7781R supply 7bit ID code for LCD module version ID															

9.2.33 NVM Control Status (RD9h)

NVM Control Status (RD9h)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	VMF_EN	0	0	0	0	0	0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Description	**VMF_EN**: ”1” = Command NVM VCOM Offset Control (RFEh) Enable. ”0” = Command NVM VCOM Offset Control (RFEh) Disable.																	

9.2.34 NVM Write Command (RDFh)

NVM Write Command (RDFh)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1
Description	NVM Write Command.																	



9.2.35 NVM Enable (RFAh)

NVM Enable (RFAh)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	PROG_MODE	0	0	0	0	1	NVM_PROG	0
Default value			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Description			**PROG_MODE**: ”1” = Enable NVM digital Function. **NVM_PROG**: ”1” =Enable NVM Function.															

9.2.36 NVM VCOM Offset (RFEh)

NVM VCOM Offset (RFEh)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	1	0	0	VMF4	VMF3	VMF2	VMF1	VMF0
Default value			0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
Description			**VCMF[4:0]**: Set VCOM voltage level for reduce the flicker issue. (Max:-0.425V Min: -2V)															

VCMF[4:0]	VCOM Output Level
00000	“VCM”-16d
00001	“VCM”-15d
|	|
01110	“VCM”-2d
01111	“VCM”-1d
10000	“VCM”
10001	“VCM”+1d
10010	“VCM”+2d
|	|
11110	“VCM”+14d
11111	“VCM”+15d

9.2.37 NVM Command Enable (RFFh)

NVM Command Enable (RFFh)																		
RS	**WRX**	**RDX**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CMD2_EN
Description			**CMD2_EN**:”1” for enable DFh function.															

10 RESET FUNCTION

The ST7781R is initialized by the RESET input. During reset period, the ST7781R is in a busy state and instruction from the MCU and DRAM access are not accepted. The ST7781R's internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, DRAM access and initial instruction setting are prohibited.

10.1.. System Function Command List

See the Instruction description. The default value is shown in the parenthesis of each instruction bit cell.

10.2.. RAM Data Initialization

The RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period.

10.3.. Note on Reset Function

- When a RESET input is entered into the ST7781R while it is in deep standby mode, the ST7781R starts up the inside logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable. For this reason, do not enter a RESET input in deep standby mode.
- When transferring instruction in either two or three transfers via 8-/9-/16-bit interface, make sure to execute data transfer synchronization after reset operation.

10.4.. Reset Timing Characteristic

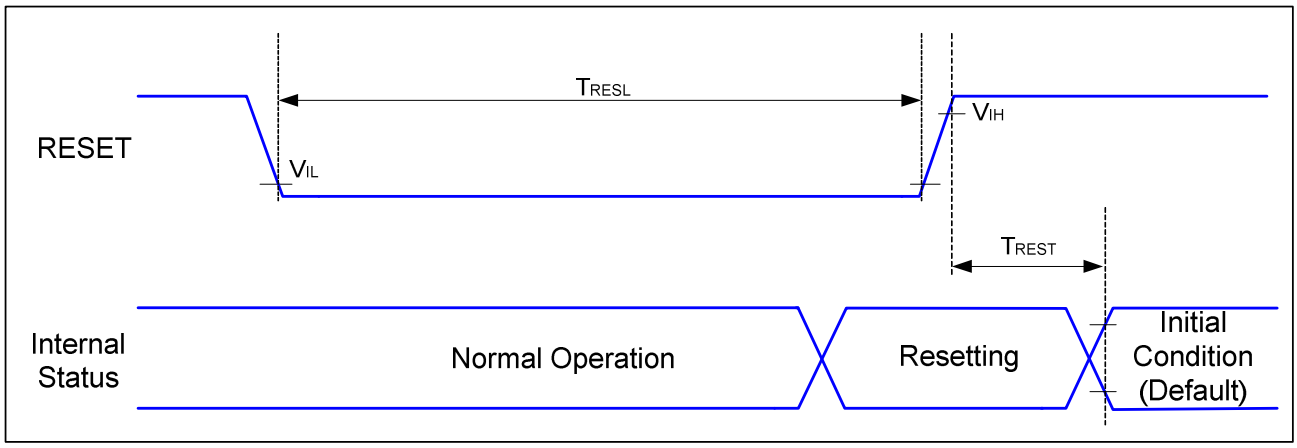


Figure 43 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
RESET	TRESL	Reset Low Level Width	1	-	ms	-
	TREST	Reset Complete Time	1		ms	

Table 10 Reset timing Characteristics

11 FMARK FUNCTION

The ST7781R outputs an FMARK pulse when the ST7781R is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

FMI[2:0]	Output Interval
000	1 Frame
001	2 Frame
011	4 Frame
101	6 Frame
Others	Setting Prohibited

Table 11 FMARK Interval

FMP[8:0]	FMARK Output Position
9'h000	0 th line
9'h001	1 st line
9'h002	2 nd line
9'h003	3 rd line
. . .	. . .
9'h174	372 th line
9'h175	373 th line
9'h176	374 th line
9'h177	375 th line

Table 12 FMARK Output Position

11.1.. FMP Setting Example

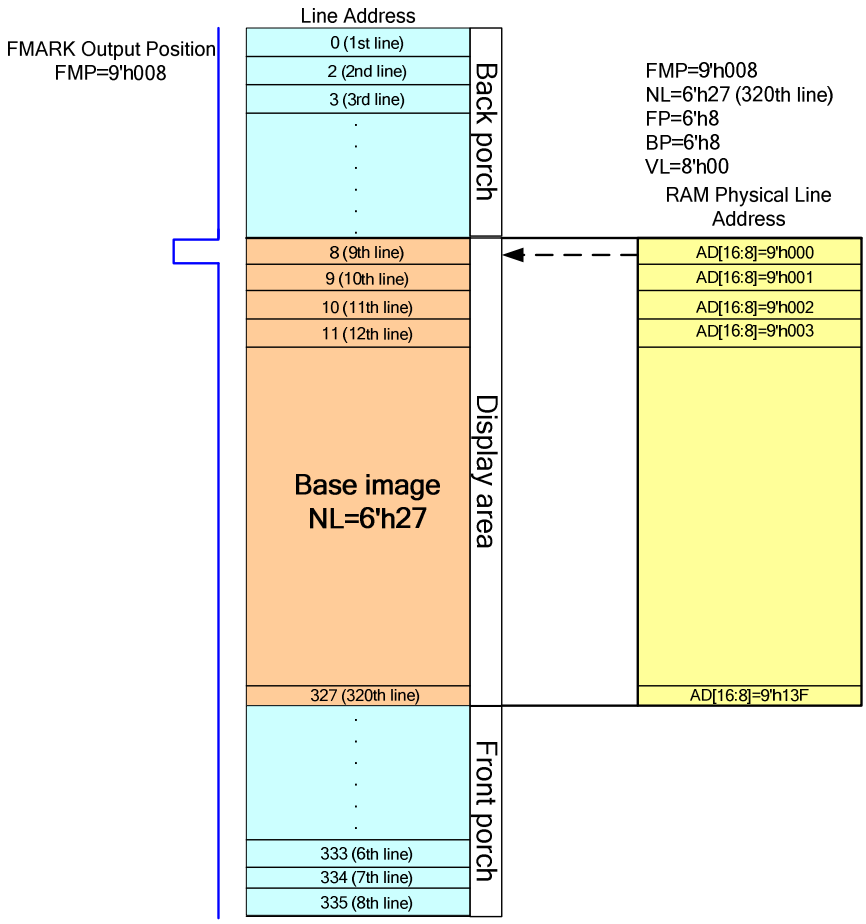


Figure 44 FMARK Setting Example

11.2.. Display Operation Synchronous Data Transfer using FMARK

The ST7781R uses FMARK signal as a trigger signal to start writing data to the internal DRAM in synchronization with display scan operation.

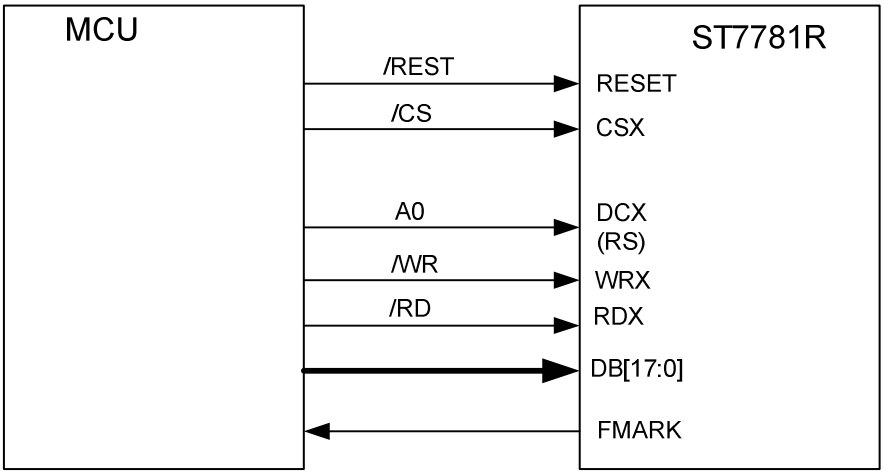


Figure 45 Display Synchronous Data Transfer Interface

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture DRAM area without causing flicker on the display. The data is written in the internal RAM in order to transfer only the data written over the moving picture display area and minimize the data transfer required for moving picture display.

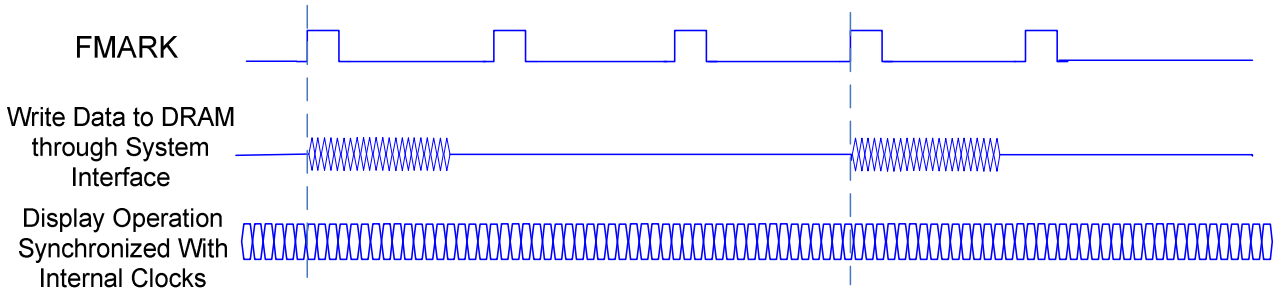


Figure 46 Moving Picture Data Transfers via FMARK Function

When transferring data in synchronization with FMARK signal, minimum DRAM data write speed and internal clock frequency must be taken into consideration. They must be more than the values calculated from the following equations.

$$Internal\ \ clock\ \ frequency\ (fosc)[Hz]$$
$$= Frame\ \ Frequency\ (\min.)[Hz] \times (DisplayPor\ \ ch(NL) + FrontPorch\ (FP) + BackPorch\ (BP)) \times 16(clocks) \times \text{var}\ iance$$
$$RAMWriteSp\ \ eed\ (\min.)[Hz] > \frac{240 \times DisplayLin\ \ es(NL)}{(FrontPorch\ (FP) + BackPorch\ (BP) + DisplayLin\ \ es(NL) - m\arg ins) \times 16(clocks) \times \frac{1}{fosc}}$$

Note: When RAM write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

Examples of DRAM writes speed and the frequency of the internal clocks are as follows.

Example:

Display size	320 RGB x 240 lines,
Total number of lines (NL)	320 lines
Back/Front porch:	14/2 lines
Frame frequency	60 Hz

Internal Clock Frequency (fosc) [Hz] = 60Hz x (320+2+14) x 16 clocks x 1.1/0.9 = 394 kHz

Note1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one FMARK cycle.

Note2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum Speed for DRAM Writing [Hz] > 240x320 / {((14+320-2)lines x 16 clocks) / 394kHz} = 5.7MHz

Note1. In this example, it is assumed that the ST7781R starts writing data in the internal DRAM on the rising edge of FMARK.

Note2. There must be at least a margin of 2 lines between the line to which the ST7781R has just written data and the line where display operation on the LCD is performed.

Note3. The FMARK signal output position is set to the line specified by FMP[8:0] bits.

In this example, DRAM write operation at a speed of 5.67MHz or more, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the ST7781R starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

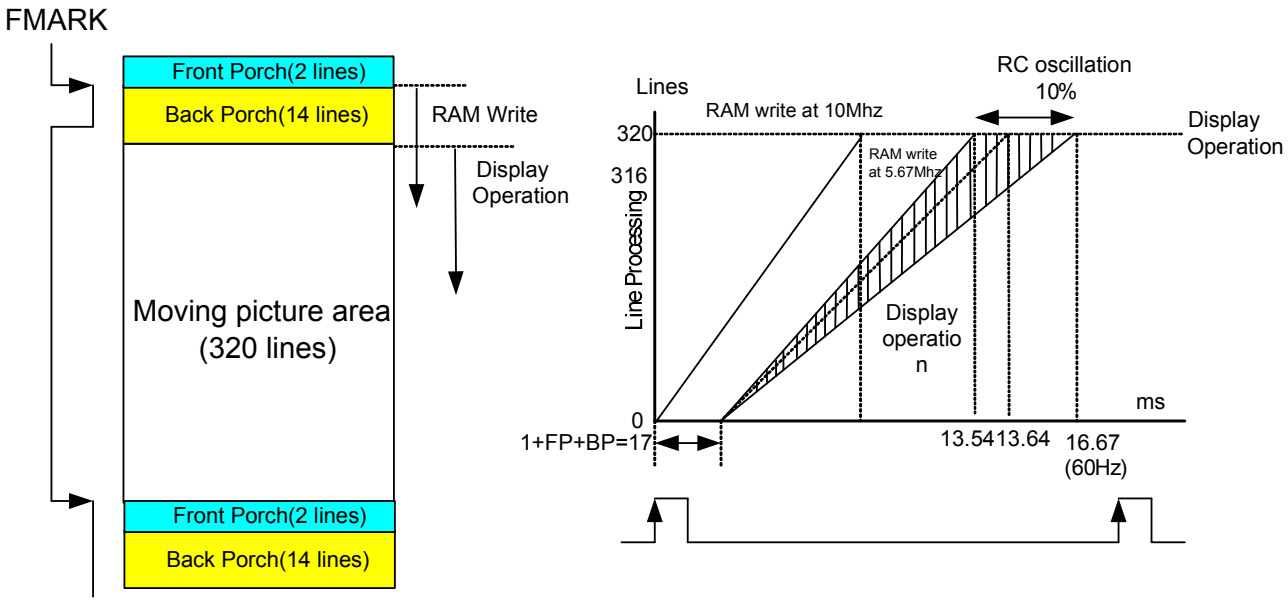


Figure 47 Write/Display Operation Timing

12 8 - COLOR DISPLAY MODE

The ST7781R has a function to display in 8 colors. In this display mode, only V0 and V63 are used and power supplies to other grayscales are turned off to reduce power consumption. In 8-color display mode, the γ-adjustment registers KP5-0[2:0], RP1-0[2:0], VRP0 [3:0], KN5-0[2:0], RN1-0[2:0], VRN1 [4:0], VRN0 [3:0], are disabled and the power supplies to V1 to V62 are halted. The ST7781R does not require DRAM data rewrite for 8-color display by writing the MSB to the rest in each dot data to display in 8 colors.

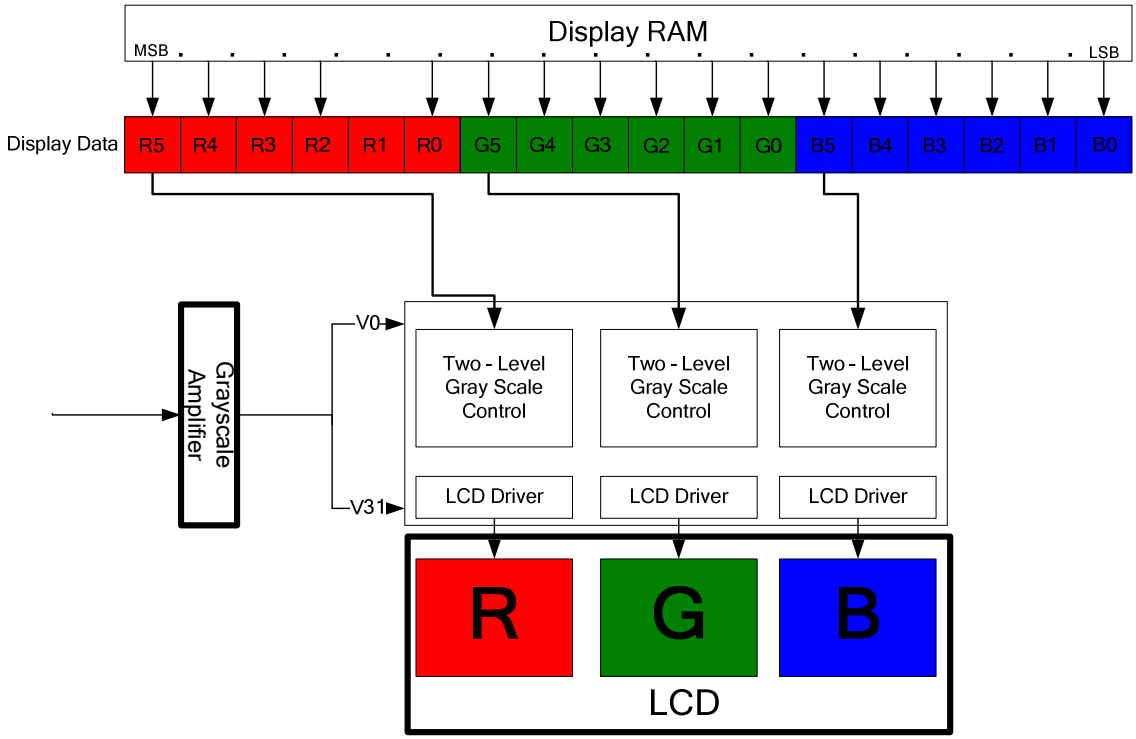


Figure 48 8-Color Display Mode

13 WINDOW ADDRESS FUNCTION

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal DRAM. The window address area is made by setting the horizontal address register (star: HAS[7:0], end HEA[7:0] bits) and the vertical address register(start: VSA[8:0], end: VEA[8:0] bits) The AM bits sets the transition direction of RAM address(either increment or decrement). These bits enable the ST7781R to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAN address map area. Also, DRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]
(Horizontal direction) 00H ≦ HSA[7:0] ≦ HEA[7:0] ≦ "EF"H
(Vertical direction) 00H ≦VSA[8:0] ≦ VEA[8:0] ≦ "13F"H
[RAM address, AD (an address within a window address area)]
(RAM address) HSA[7:0] ≦AD[7:0] ≦HEA[7:0]
VSA[8:0] ≦AD[15:8] ≦VEA[8:0]

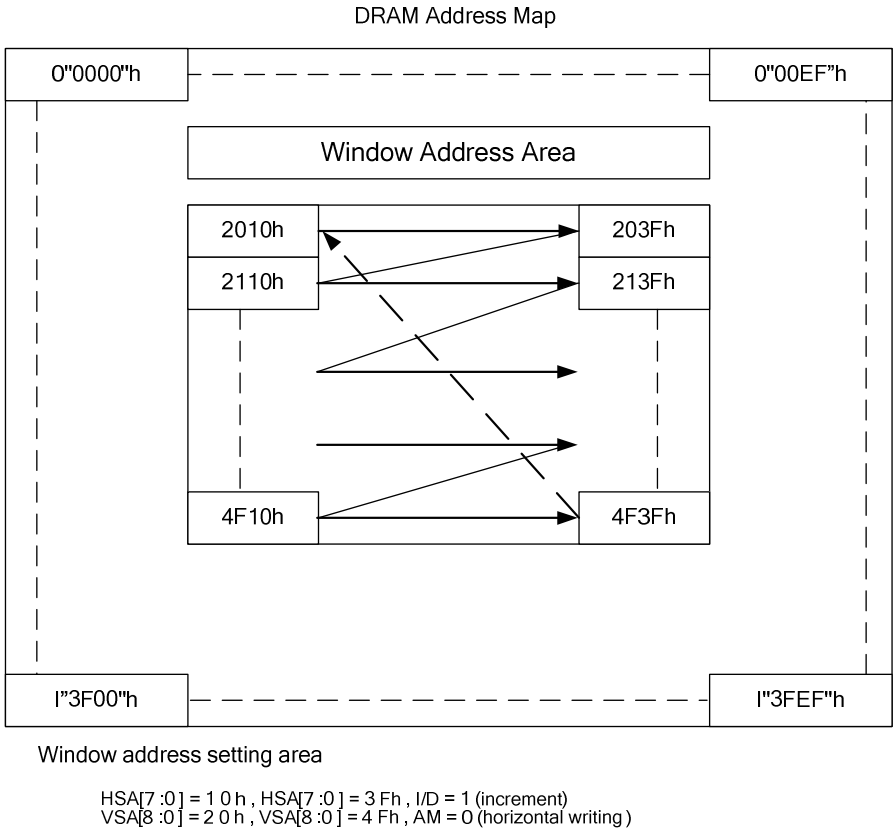


Figure 49 DRAM Access Window Map

14 GAMMA CORRECTION

ST7781R incorporate the γ- correction function to display 262,244 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine- adjustment registers for positive and negative polarities, to make ST7781R available with liquid crystal panels of various characteristics.

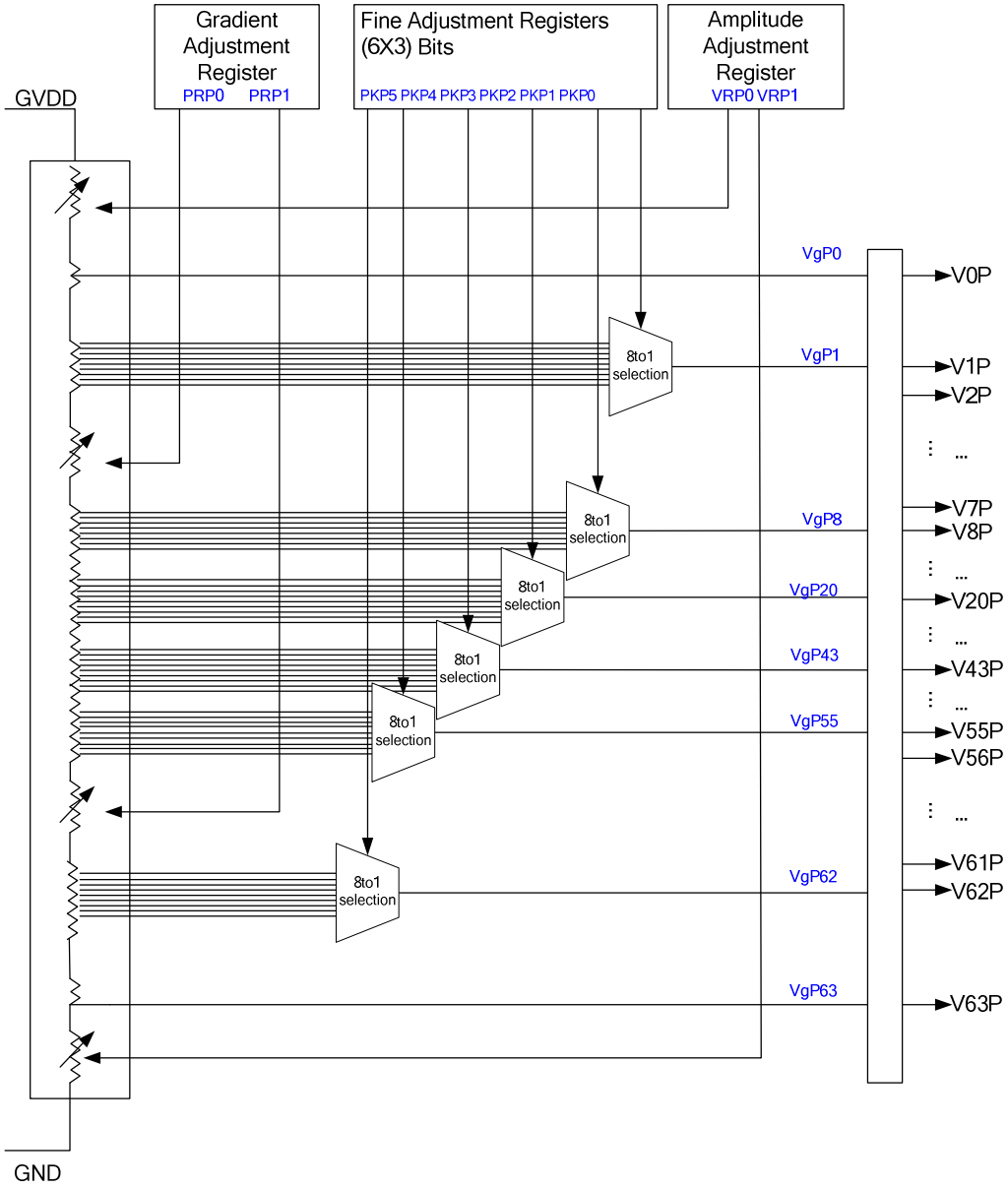


Figure 50 Grayscale Voltage Generation (Positive)

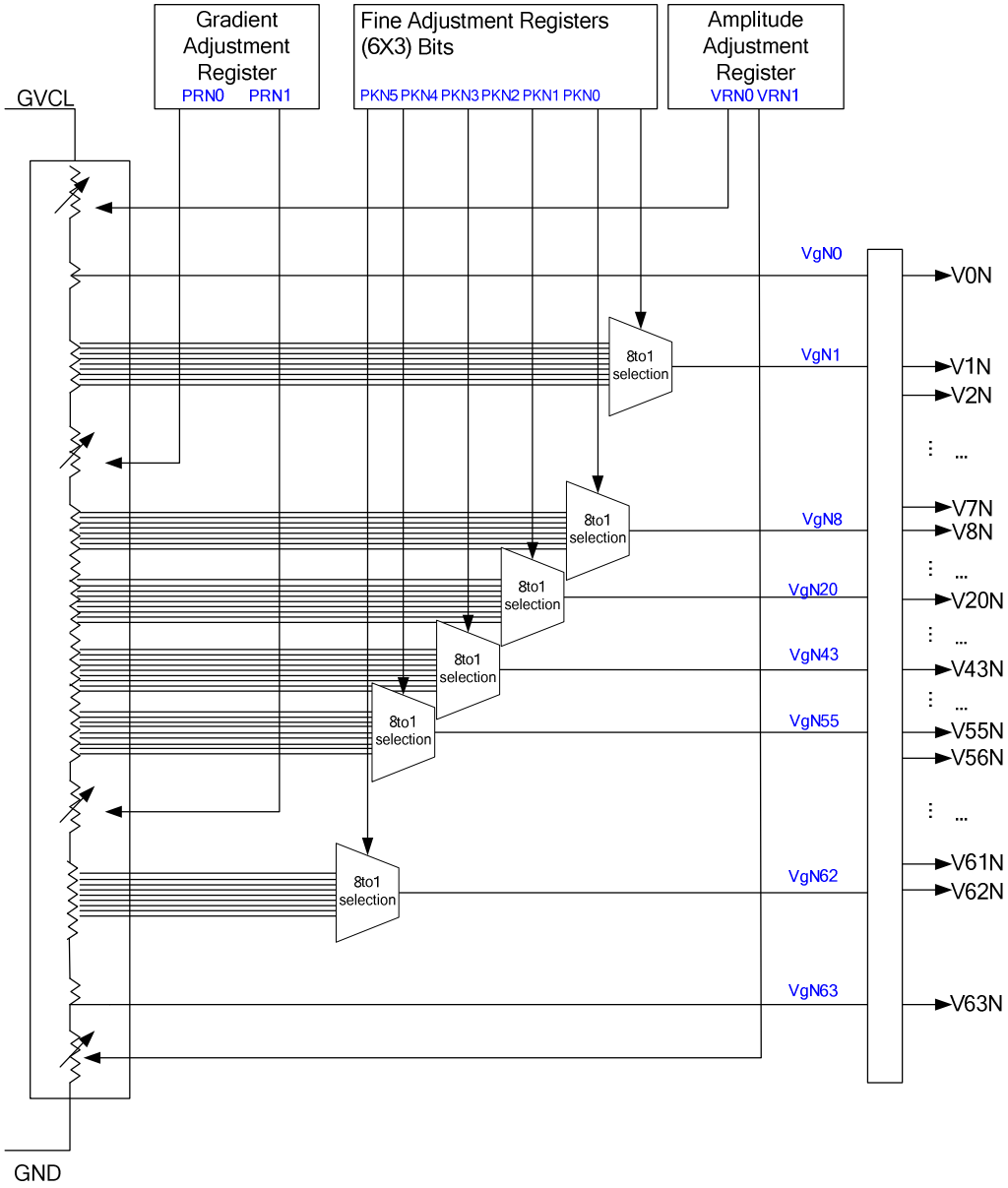


Figure 51 Grayscale Voltage Generation (Negative)

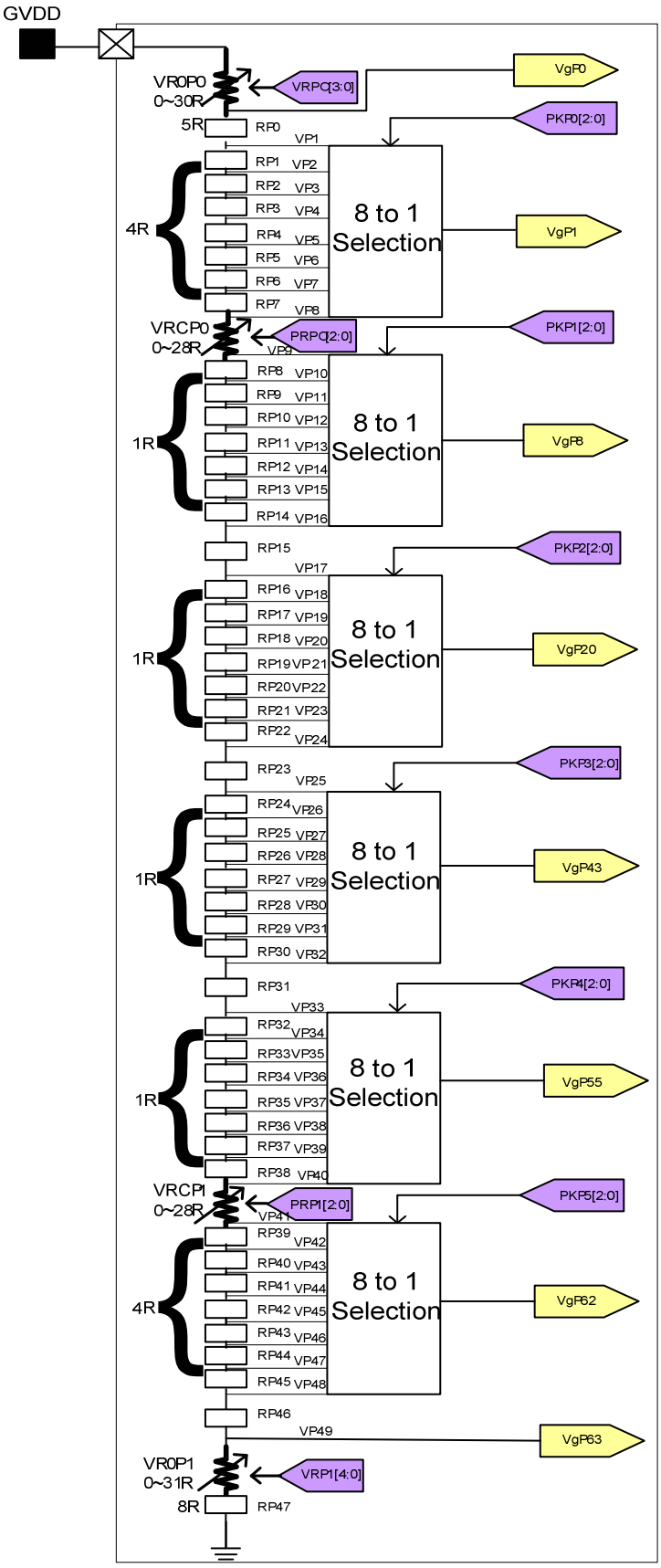


Figure 52 Grayscale Voltage Block (Positive)

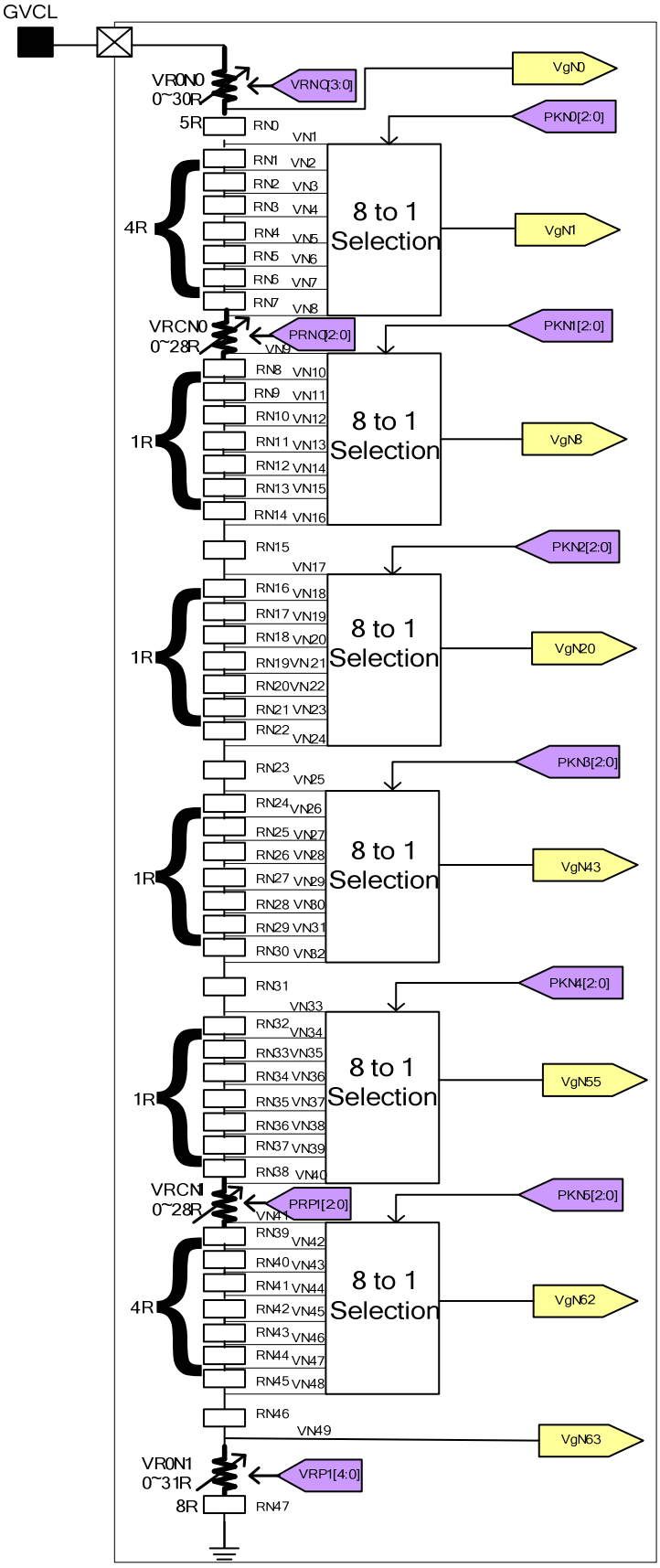


Figure 53 Grayscale Voltage Block (Negative)

1. Gradient Adjustment Registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude Adjustment Registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/ VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and the bottom of the ladder resister are adjusted.

3. Fine Adjustment Registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage level, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

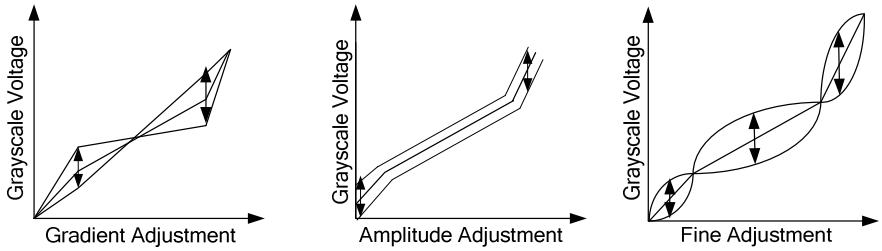


Figure 54 Gamma curve adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient Adjustment	PRP0[2:0]	PRN0[2:0]	Variable Resistor VRCP0,VRCN0
	PRP1[2:0]	PRN1[2:0]	Variable Resistor VRCP1,VRCN1
Amplitude Adjustment	VRP0[3:0]	VRN0[3:0]	Variable Resistor VROP0,VRON0
	VRP1[4:0]	VRN1[4:0]	Variable Resistor VROP1,VRON1
Fine Adjustment	KP0[2:0]	KN0[2:0]	8-to-1 Selector (Voltage Level of Grayscale1)
	KP1[2:0]	KN1[2:0]	8-to-1 Selector (Voltage Level of Grayscale8)
	KP2[2:0]	KN2[2:0]	8-to-1 Selector (Voltage Level of Grayscale20)
	KP3[2:0]	KN3[2:0]	8-to-1 Selector (Voltage Level of Grayscale43)
	KP4[2:0]	KN4[2:0]	8-to-1 Selector (Voltage Level of Grayscale55)
	KP5[2:0]	KN5[2:0]	8-to-1 Selector (Voltage Level of Grayscale62)

Table 13 Register Description

14.1.. Ladder Resistors and 8-to-1 Selector Block Configuration

The reference voltage generation block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-10-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristic of panels.

14.2.. Variable Resistors

ST7781R uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient Adjustment		**Amplitude Adjustment (1)**		**Amplitude Adjustment (2)**	
PRP(N)0/1[2:0] Register	**VRCP(N)0 Resistance**	**VRP(N)0[3:0] Register**	**VROP(N)0 Resistance**	**VRP(N)1[4:0] Register**	**VROP(N)1 Resistance**
000	0R	0000	0R	00000	0R
001	4R	0001	2R	00001	1R
010	8R	0010	4R	00010	2R
011	12R	:	:	:	:
100	16R	:	:	:	:
101	20R	1101	26R	11101	29R
110	24R	1111	28R	11110	30R
111	28R	1111	30R	11111	31R

Table 14 Resistance Adjustment

14.3.. 8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine Adjustment Registers and Selected Voltage						
Register	**Selected Voltage**					
KP(N)[2:0]	**VgP(N)1**	**VgP(N)8**	**VgP(N)20**	**VgP(N)43**	**VgP(N)55**	**VgP(N)62**
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 15 Fine Adjustment Registers and Selected Voltage

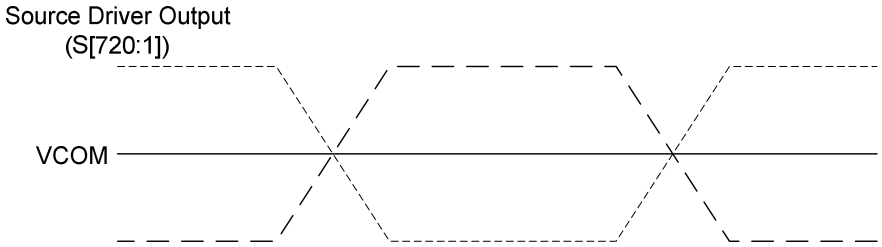


Figure 55 Relationship between Source Output and VCOM

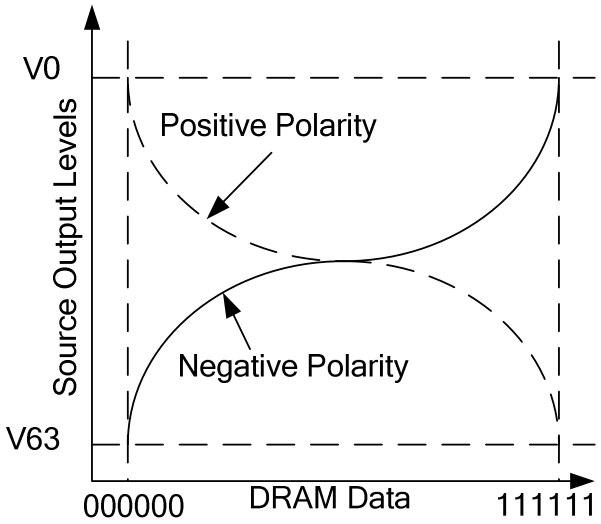


Figure 56 Relationship between DRAM Data and Output Level

15 APPLICATION

15.1.. Configuration of Power Supply Circuit

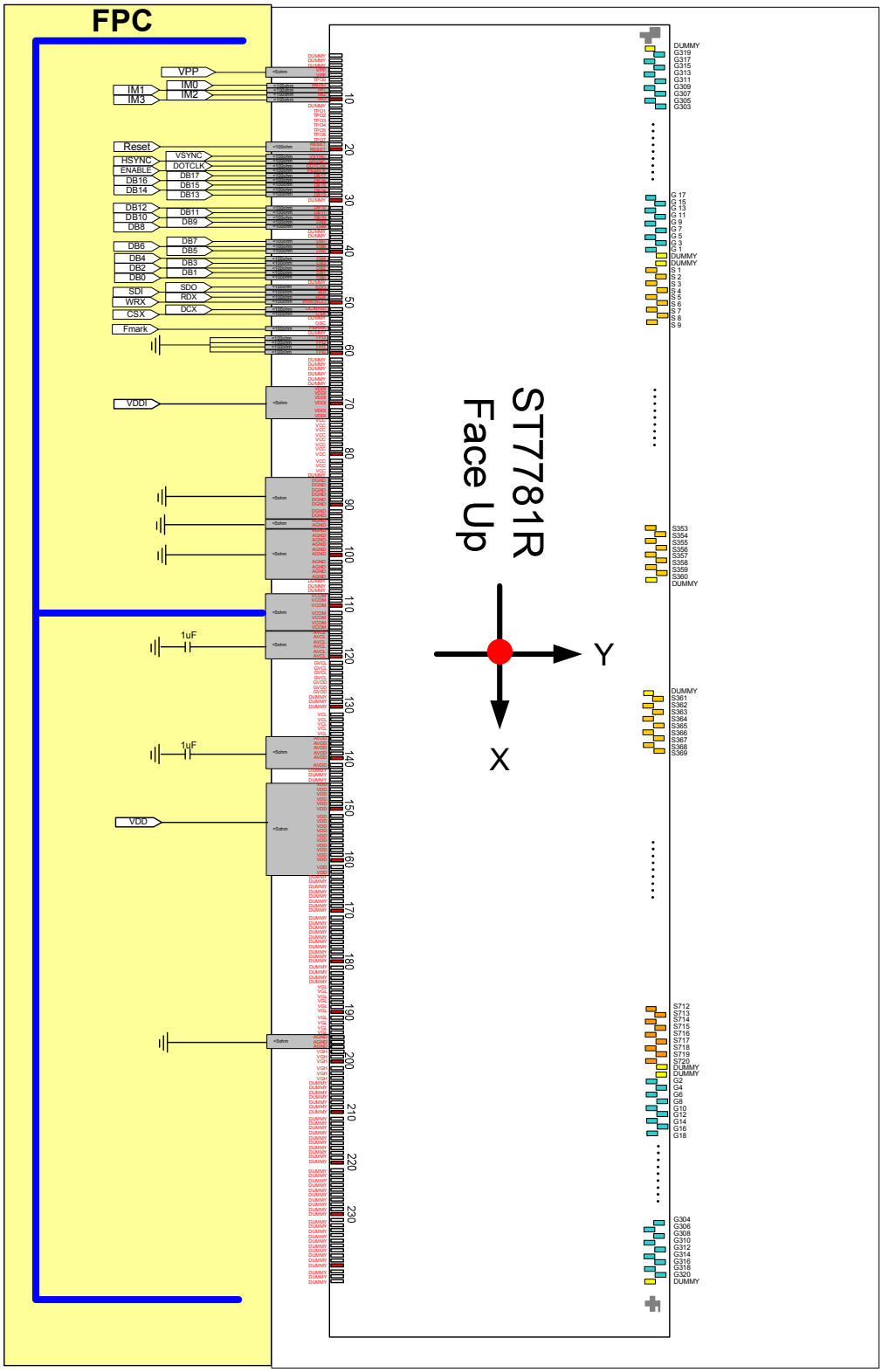


Figure 57 Power Supply Circuit Block

The following table shows specifications of external elements connected to the ST7781R power supply circuit.

Items	Recommended Specification	Pin Connection
1 µF Capacity	6.3 V	AVCL, AVDD

Table 16 Outside Components

15.2.. Standby Mode

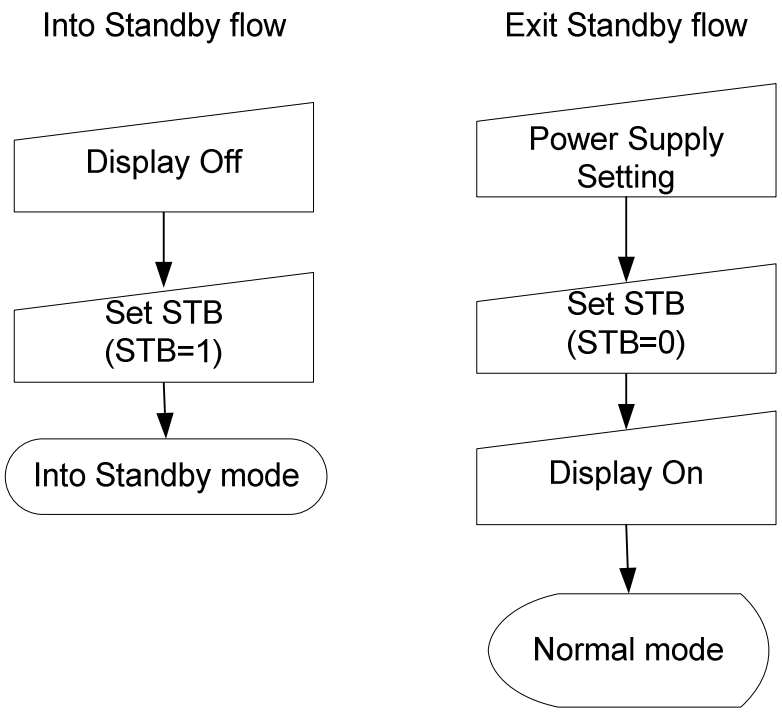


Figure 58 Standby Mode Register Setting Sequence

15.3.. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, circuits and operational amplifiers depends on external resistance and capacitance.

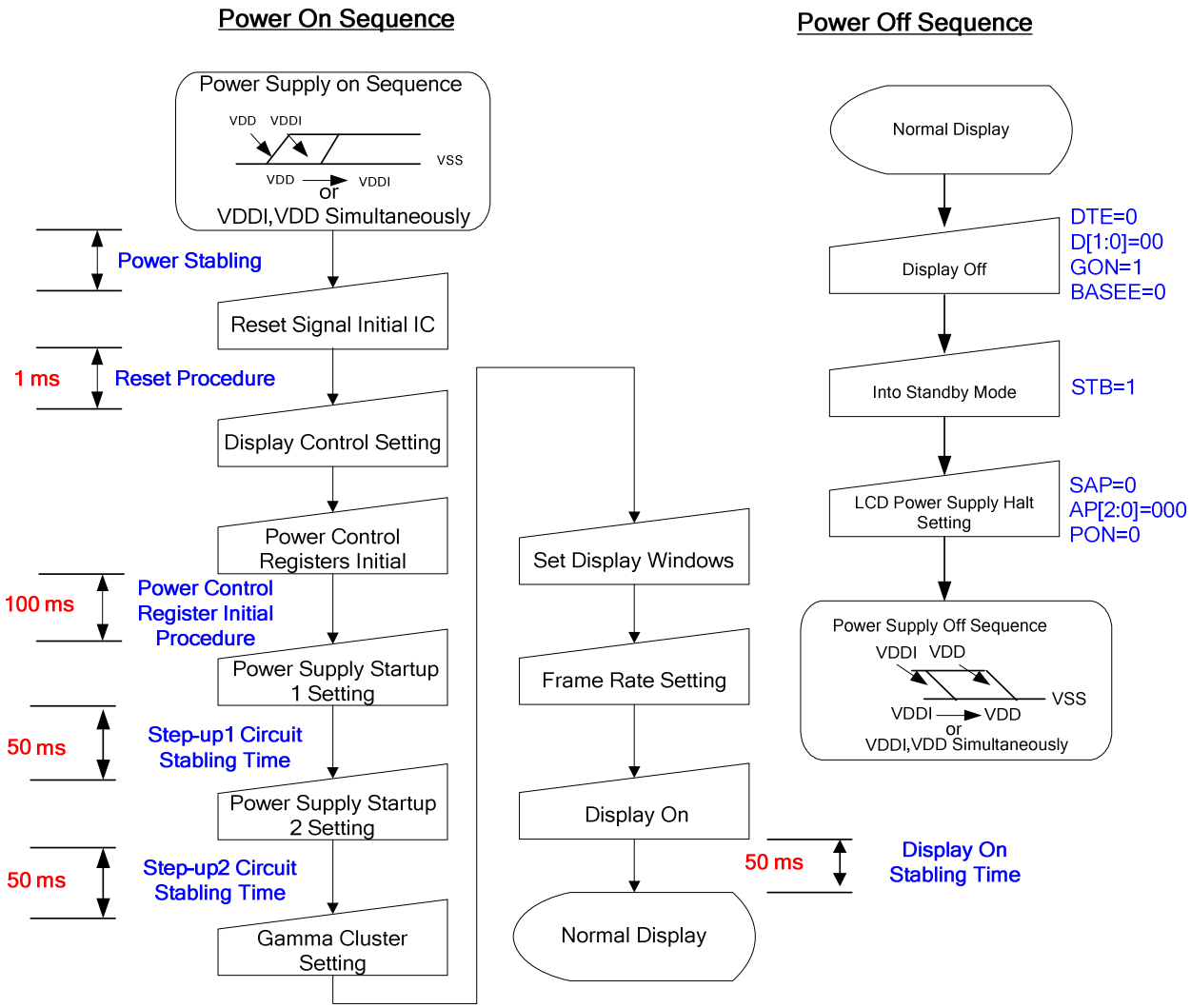


Figure 59 Power Supply ON/OFF Sequence

15.4.. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ST7781R are as follows.

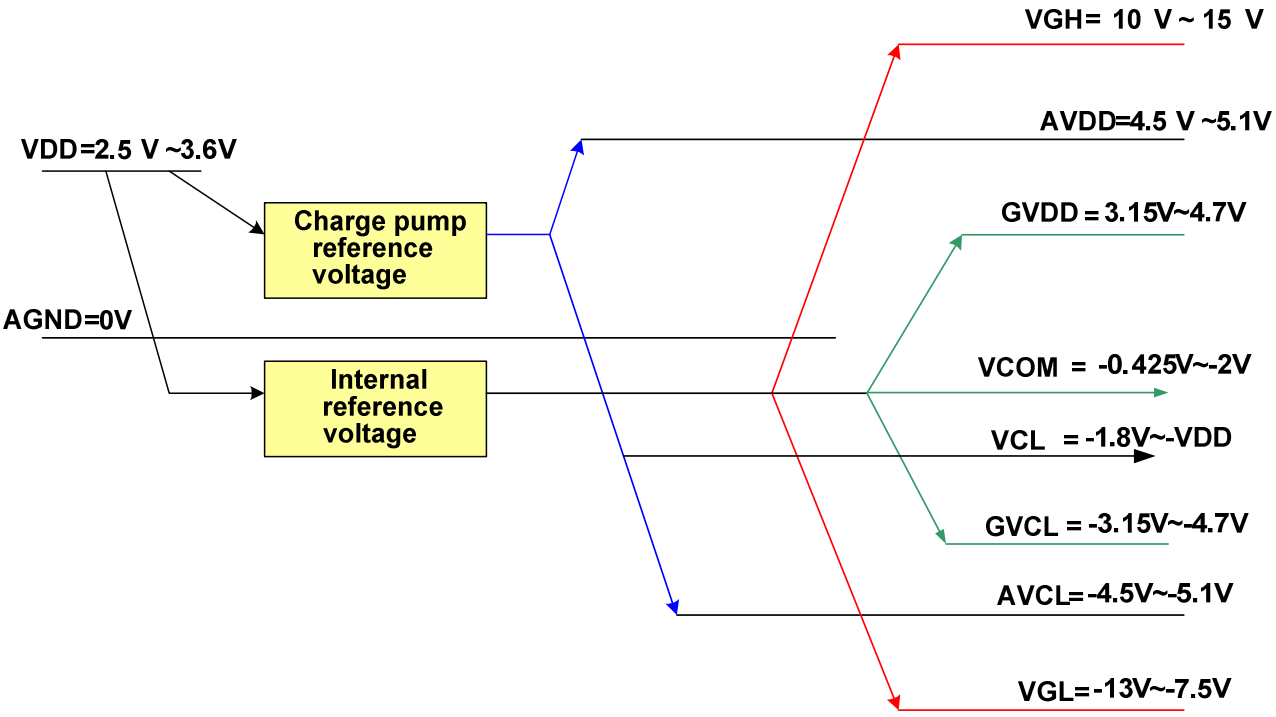


Figure 60 Power Booster Level

15.5.. Applied Voltage to the TFT panel

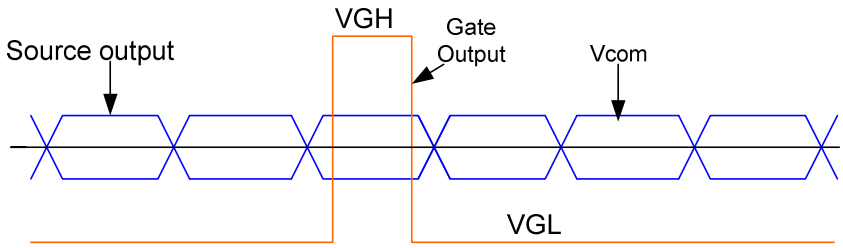


Figure 61 Voltage Output to TFT LCD Panel

15.6.. Partial Display Function

The ST7781R allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers. The following example shows the setting for partial display function:

Base Image Display Setting	
BASEE	0
NL[5:0]	6'h27
Partial Image 1 Display Setting	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080
Partial Image 2 Display Setting	
PTDE1	1
PTSA1[8:0]	9'h020
PTEA1[8:0]	9'h02F
PTDP1[8:0]	9'h0C0

Table 17 Partial Setting Example

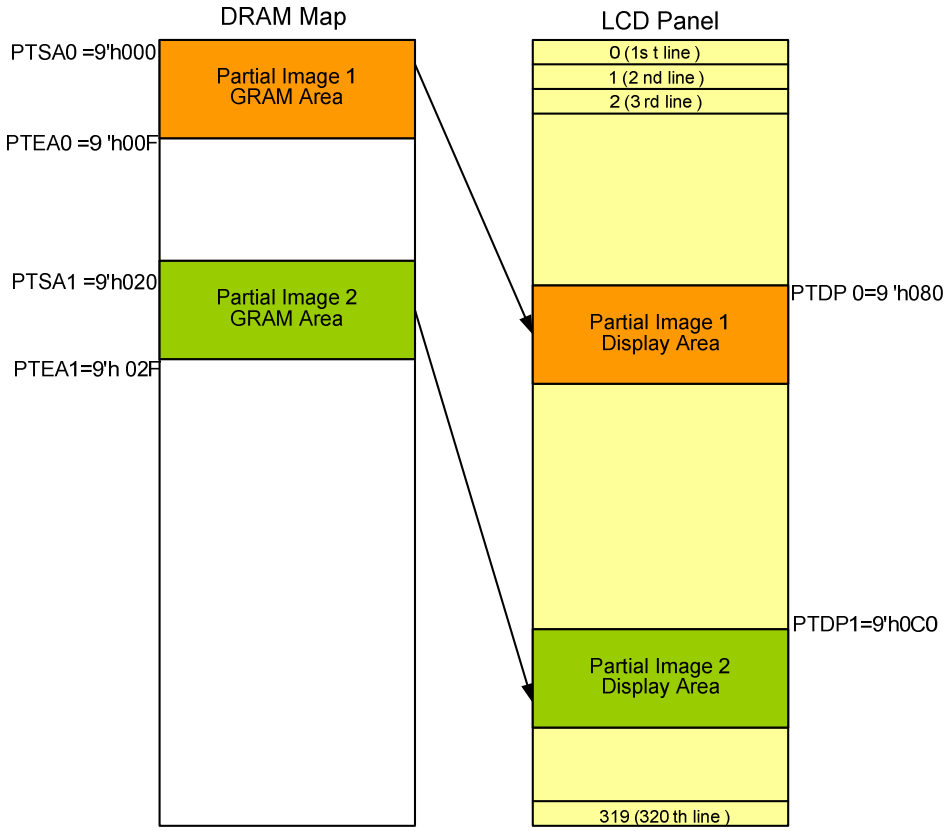


Figure 62 Partial Display Example

15.7.. Resizing Function

ST7781R supports resizing function (x1/2, x1/4), which is performed when writing image data to DRAM. The resizing function is enabled by setting a window address area and the RSZ bit which represents the resizing factor (x1/2, x1/4) of image. The resizing function allows the system to transfer the original-size image data into the DRAM with resized image data.

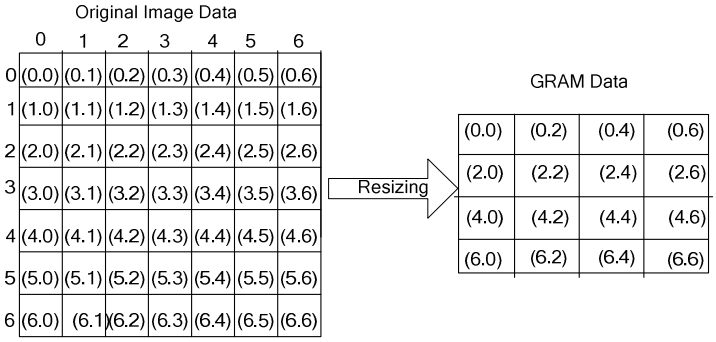


Figure 63 Data Transfer in Resizing Mode

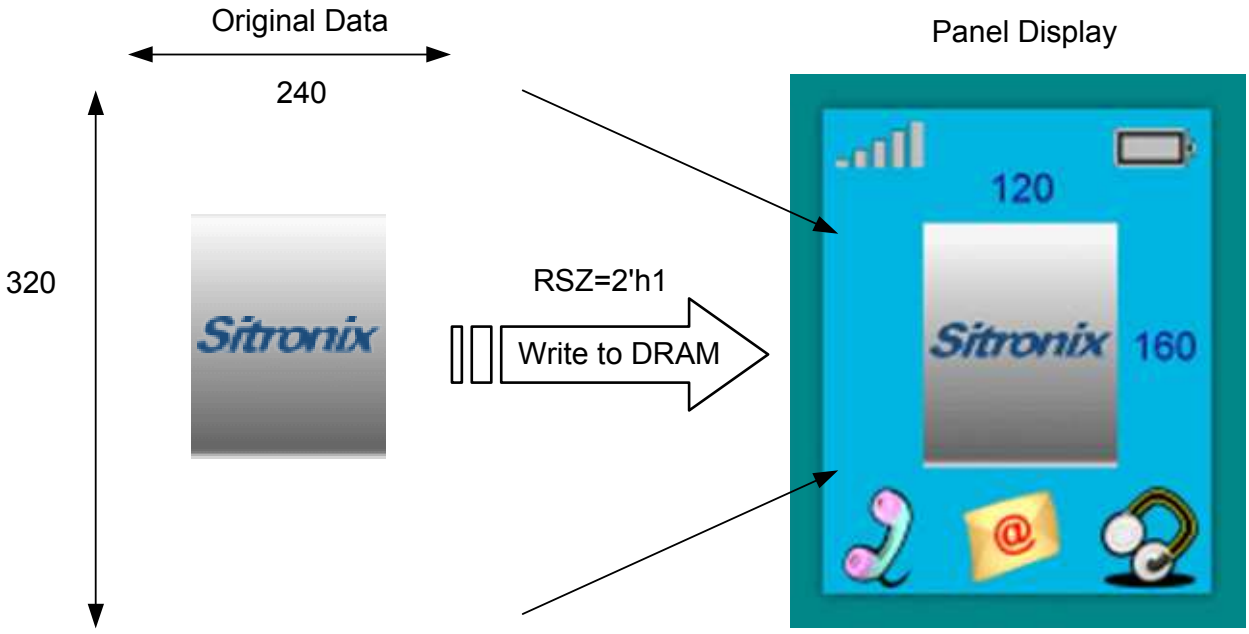


Figure 64 Resizing Example

Original Image Size (X × Y)	Resized Image Resolution	
	1/2 (RSZ=2'h1)	1/4 (RSZ=2'h3)
640 × 480	320 × 240	160 × 120
352 × 288	176 × 144	88 × 72
320 × 240	60 × 120	80× 60
176 × 144	88 × 72	44× 36
120 × 160	60× 80	30 × 40
132 × 132	66 × 66	33 × 33

Table 18 Resized Image Resolution

The RSZ bit sets the resizing factor of an image. When setting a window address area in the internal DRAM, the DRAM window address area must fit the size of resized image. The following examples show the resizing setting.

Original image data number in horizontal direction		X
Original image data number in Vertical direction		Y
Resizing Ration		1/N
Resizing Setting	RSZ	N-1
Remainder pixels in horizontal direction	RCH	H
Remainder pixels in vertical direction	RCV	V
DRAM writing start address	AD	(X0, Y0)
DRAM window setting	HAS	X0
	HEA	X0+dX-1
	VSA	Y0
	VEA	Y0+dY-1

Table 19 Resized Coefficient

16 REVISION HISTORY

Version	Date	Description
Draft	2009/09/01	Draft
0.1	2009/12/23	Page 10: VCOM voltage description Page 11: Au bump height 15→12μm Page 37: SDI description Page 38: VPP description Page86: Register default setting Page117: VGH, VGL description Page 118: RB0h VGH and V25 description Page 119: RB3h description Page120: AVCL description Page 125: RB0h Vcom offset description Page 146: Volotage description Page 150: NVM Flow
0.2	2010/04/20	Add timing values Add power consumption Modify DC characteristics description Page40: Maximum allowable resistance Page44: Modify VO and VIN description
1.0	2010/09/09	Page 45: Modify DC Characteristics description Page 46: Modify Power Consumption notes description Page 77: Modify start byte format description